A 3-Level PWM ADSL2+ CO Line Driver

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***Abstract*- A PWM ADSL2+ line driver with 2.2MHz signal bandwidth is realized in a 3 metal, 2 poly 0.35µm CMOS process. A low 8.832MHz switching frequency is used with filtering in the feedback path to suppress aliasing. Signal processing and triangular wave generation are combined in the forward integrators. The driver delivers 100mW to a 100Ω line with an MTPR less than -52 dB. Active area is 3mm^2.**

I. Introduction

Conventionally, the DSL line driver at the central office (CO) is implemented as a bipolar class-AB amplifier. However, linear amplification of the Discrete Multi Tone (DMT) signal is very power inefficient because the signal hovers around zero with occasional peaks due to the large peak-to-rms ratio (PAR). Recently, a self-oscillating CMOS amplifier was reported to improve efficiency [1]. The work presented here significantly differs from [1] in terms of both architecture and CMOS technology. The chip area is only 3mm^2 in a 0.35µm 2P3M process compared to 8.2mm^2 in a 0.13µm 1P6M process [1].

To deliver 20dBm of power in an ADSL2+ system the peak line voltage is about 18V. As technology limits supply voltage, a step-up transformer must be used. For a given technology it can be shown that class-D power amplifier efficiency degrades as transformer ratio is increased and/or supply voltage is reduced. Furthermore, step-up ratios larger than 2.5 become unpractical, as it degrades transformer bandwidth and SNR of the signal received from the Customer Premise Equipment (CPE). Therefore it is necessary to choose a process that supports high voltage. Although some CMOS processes offer high-voltage DMOS transistors, the DMOS devices are generally much slower than the CMOS devices. Further such processes are more expensive than conventional CMOS. Here we use a mainstream 0.35µm CMOS technology with thick oxide 5V transistors that can support a 10V supply voltage when stacked. Core devices are used to perform low-power signal processing. Three-level (+1, 0, -1) differential Pulse Width Modulation (PWM) is chosen to better track the predominantly low-level DMT signal. The switching frequency of each bridge half is only 8.832MHz compared to the 25MHz self-oscillation frequency of [1]. The lower switching rate is favorable for lower power consumption.

Class-D PWM amplifiers are common in audio applications. The triangle or ramp rate for audio is generally more than a factor of ten times the signal bandwidth. For broadband applications such large oversampling cannot be used. Section II of the paper discusses the challenges related to the use of a relatively low switching rate. A 3-level PWM system offers some challenges that are not present in a 2-level PWM [3]. Effect of duty cycle error and integrator offsets are highlighted in section III. A local feedback scheme to mitigate these errors is discussed. Extensive measurement results are reported in section IV.

II. System Design

The driver's block diagram is shown in Figure 1. True and complementary versions of the analog input signal are compared with a triangular waveform to obtain naturally sampled PWM signals, driving the H-bridge power stage.

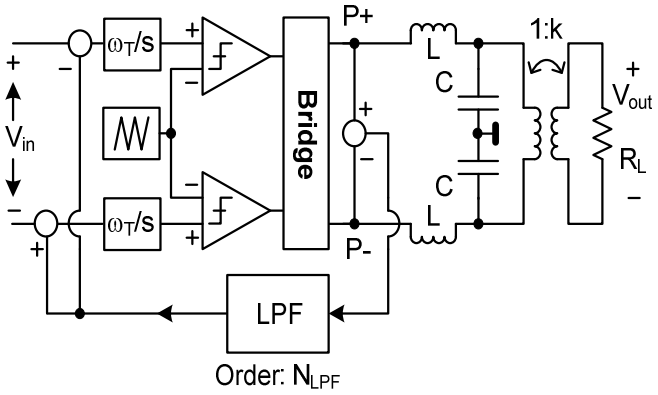

Figure 1: Block diagram of 3-level PWM line driver.

The differencing operation in the bridge results in a 3-level PWM signal. Feedback minimizes non-linearity introduced in the power stage. A low-pass filter (LPF) reduces aliasing by suppressing the high-frequency Bessel components that feed back into the comparators. The integrators in the forward path provide the in-band distortion "shaping". The LC filters suppress high frequency energy and increase the load impedance seen by the power stage at the switching frequency.

The frequency of the triangular signal $f_{triangle}$ should be minimal to reduce switching losses and dissipation in the low-level signal processing section. However, a low switching frequency leads to an increase in distortion due to aliasing [2]. Aliasing occurs when high-frequency Bessel components located around multiples of $f_{triangle}$ feed back into the

comparators that perform natural sampling. Thus, energy folds into the signal band and results in distortion, even in an ideal system. Aliasing depends strongly on the transfer function from comparator output back to its input, as shown for 2-level PWM in [2]. As this transfer also affects the distortion "shaping", the overall goal is to find a loop transfer that minimizes aliasing while maximizing shaping. Figure 2 shows theoretical and simulated HD3 due to aliasing for a 3-level PWM closed loop system. It assumes a single integrator with various feedback low-pass filter orders N_{LPF}; all components are ideal. Theoretical results are obtained by extending the theory in [2] to 3-level PWM and confirmed with simulation using Simulink. The integrator f_T and LPF cutoff frequencies are chosen such that the signal bandwidth is 2MHz in all cases.

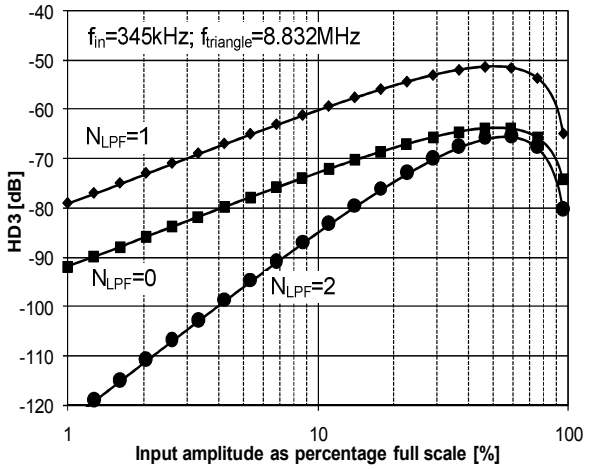

Figure 2: HD3 due to aliasing: theory and simulation (dots).

As shown in figure 2, theory and simulation match closely. At very low and very high input amplitudes the distortion due to aliasing is less due to the decrease in energy of the high-frequency Bessel components in the 3-level PWM signal. Surprisingly, a single integrator without any LPF (N_{LPF}=0) outperforms the combination of integrator and 1st-order feedback filter. Even though the 1st-order filter reduces high-frequency Bessel components, it worsens aliasing. This is because both magnitude and phase transfer from modulator output back to its input play a crucial role in the amount of aliasing [2]. The 2nd-order filter provides a better solution, particularly at medium and low input levels. As the DMT signal hovers around zero most of the time, the system benefits from having a 2nd-order filter in the feedback path.

Figure 3 shows the simulated Multi-Tone-Power-Ratio (MTPR) due to aliasing in a closed-loop 3-level PWM system with $f_{triangle}$=8.832MHz and signal BW=2.2MHz, again assuming the system is ideal. The out-of-band suppression of the LC filter is not included. The plot is obtained by taking the average output power spectrum over 40 random DMT symbols, each with PAR=5.6. The input signal is applied at 90% full-scale. Again the 2nd-order feedback filter is the best option, both in- and out-of-band. LPF orders higher than two offer no further improvement in aliasing. Neither does adding more feed forward integrators, which become useful only when higher-order shaping is needed to further suppress the non-linearity of the power stage.

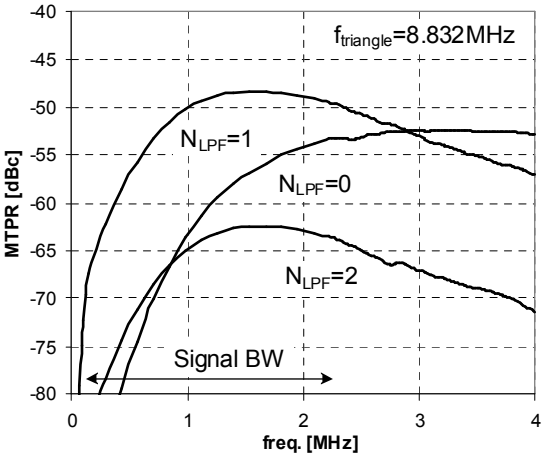

Figure 3: Simulated avg. MTPR due to aliasing; PAR=5.6.

III. Circuit Details

Based on these considerations, the block diagram of Figure 1 is implemented as shown in Figure 4. The design is fully differential and shown here as single ended for simplicity. To compare the differential integrator output with a triangular reference requires a 4-input differential differencing input stage with rail-to-rail input common-mode range. Such a comparator would have a slow response time. To overcome this, triangle generation and subtraction are performed in the integrator itself, allowing the comparator to be a zero crossing detector with well defined input common mode level [3].

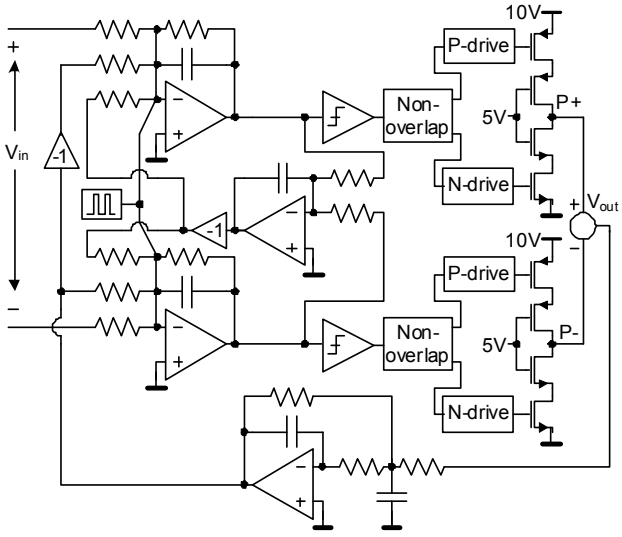

Figure 4: Single-ended representation of line driver.

A charge-pump supplies a square current to the integrator which generates the triangle. Any current mismatch or duty cycle offset can be modelled as an input offset voltage to the integrators. Since the overall feedback senses the differential output, whereas the triangle is a common-mode signal, it can not correct for this offset, unlike the case of two-level PWM in [3]. Therefore DC feedback is applied locally to both integrators. Each forward integrator with the common DC feedback path forms a Tow-Thomas biquad. The biquad's band-pass output matches the response of an ideal integrator for frequencies above 100kHz, which is the band of interest.

The 2nd-order LPF in the feedback path is implemented as a Rauch biquad based on a single differential OpAmp. It offers good common mode suppression and performs a level shift from the 10V bridge section to the 3.3V signal processing part.

The technology's highest allowable supply voltage has to be used to achieve high efficiency. A simple stack of two 5V transistors for both n- and p- devices allows for a supply voltage of 10V for the bridge. The gates of the cascode devices are fixed at 5V. As the devices do not experience maximum gate-to-source and drain-to-source voltages at the same instant, hot carrier effects are less. In a conventional CMOS process with a p-substrate, the p-channel devices can be placed in separate n-wells. As a result the 10V supply appears across two drain-to-body diodes and junction breakdown is not an issue. Unfortunately, the n-channel devices have no isolated wells and the entire 10V appears across a single drain-to-substrate diode of the cascode device. The breakdown voltage of this process is just above 10V.

IV. Experimental Results

Figure 5 shows measured waveforms in one half of the bridge. It shows the input sinusoidal signal, the triangle wave and the 2-level PWM signal of one bridge half. Together with the 2-level PWM signal of the other bridge half this forms the 3-level PWM signal in differential mode. The triangle wave is measured through an on-chip test buffer. As shown the average level of the triangular wave follows the input sinusoid allowing the comparator to be a zero crossing detector as mentioned earlier. Clearly the PWM signal switches whenever the triangle crosses the zero level, confirming the correct functionality of the circuit. Voltage spikes in the PWM signal caused by bond wire inductance can also be seen. These spikes may cause temporary breakdown of the drain-to-substrate junction of the n-channel device resulting higher non-linearity and higher power consumption.

A Multi-Tone Power Ratio (MTPR) test is performed to determine the non-linearity of the ADSL2+ line driver. A Discrete Multi Tone (DMT) waveform is a signal consisting of multiple discrete frequency components. In case of an MTPR test, this waveform contains missing frequency components, or spectral notches. The MTPR is defined as the ratio of the power in the spectral notches to the power of the individual frequency components. Figure 6 shows the measured DMT spectrum at the line while delivering 100mW of power to a 100Ω line through a 1:2.3 step-up transformer. The signal has a PAR of 5 giving a peak line voltage of 18V. The resulting worst-case MTPR is -52dB. Although acceptable, it is worse than indicated by system and transistor level simulations. We believe that the junction breakdown issue mentioned earlier to be adversely affecting MTPR.

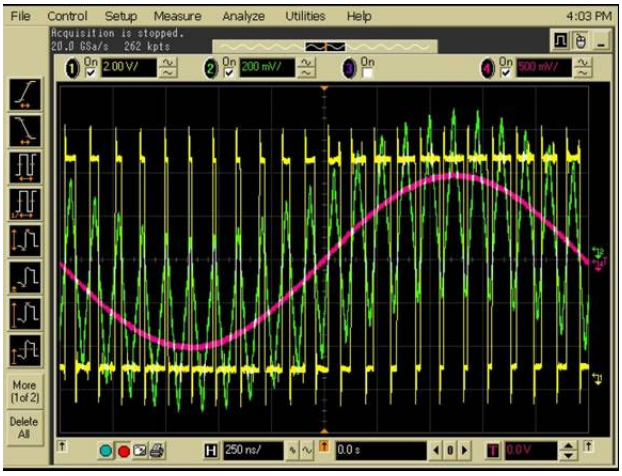

Figure 5: Measured line driver waveforms in one bridge half.

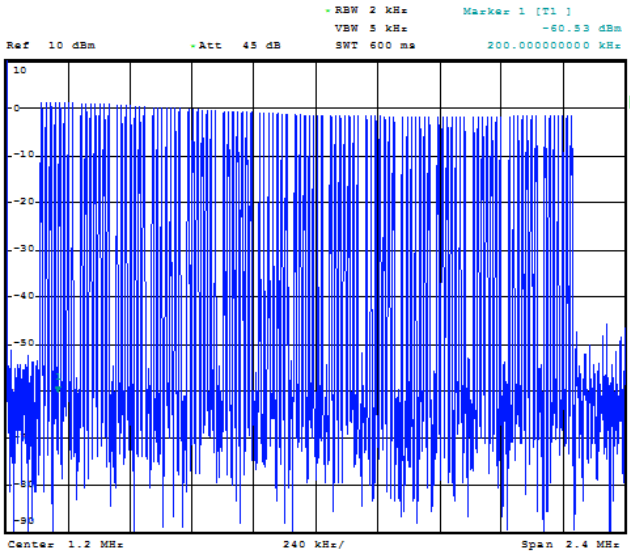

Figure 6: Measured DMT spectrum at line;
P_{line}=100mW; PAR=5.

Figure 7 shows the measured ADSL2+ downstream data rate in as a function of line length. The measurement was taken by connecting a CO board including the class D line driver to a CPE device, through a Spirent line simulator box. As in any DSL setup the line attenuation increases dramatically as the

length increases, especially at higher frequencies, causing the system to reduce the bit loading of the high-frequency DMT tones. Also the system automatically increases line power at long loop lengths, to compensate for the increased attenuation and thus loss in SNR. The downstream data rate is measured by the CPE itself and obtained through an Ethernet connection between PC and CPE. Existing firmware was used in CO and CPE; by optimizing firmware for this particular line driver the data rate can be increased somewhat more.

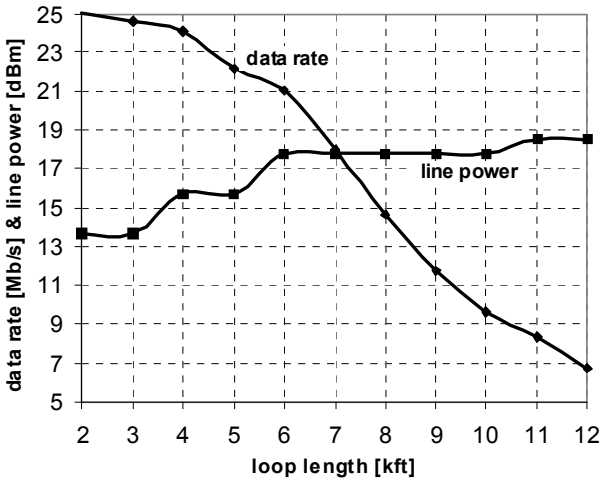

Figure 7: Measured data rate and line power as function of loop length.

Table I summarizes measured performance data.

Technology	0.35µm CMOS, 3 metal, 2 poly
Supplies	10V, 5V, 3.3V
Transformer ratio	1:2.3
R_{load} secondary	100Ω
Signal bandwidth	2.2MHz
PAR	>5
Switching frequency	8.832MHz
Peak line voltage	18V
MTPR	<-52dB
Power consumption (*including load power*)	525mW @ 100mW onto line
Active area	3mm^2

Table I: Performance summary.

Figure 8 shows a die photograph. Bonding pads are integrated into the layout of the high current devices of the bridge section. Series resistance is further reduced with the help of multiple bond wires.

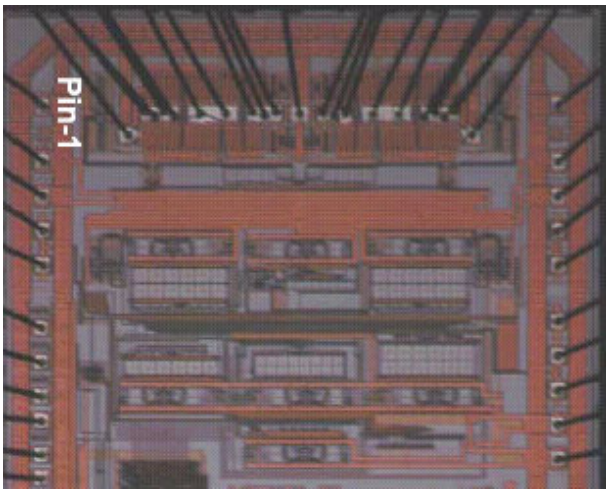

Figure 8: Die photograph

V. Conclusion

This paper discusses the design of a 3-level PWM 0.35µm CMOS class-D amplifier for broadband (>2.2MHz) signals. Distortion caused by aliasing due to the low ratio of four between triangular frequency and signal bandwidth is discussed and reduced by selecting optimal filtering in the feedback path. Circuit techniques to improve the response time of the comparator and offset compensation scheme to generate linear triangular signals are also discussed. The circuit is implemented in an inexpensive 0.35µm mainstream CMOS process without any extra processing steps. Measurement results including data rate measurements in an actual DSL set-up are reported.

References

[1] B. Serneels, M. Steyaert, W. Dehaene, "A 237mW aDSL2+ CO Line Driver in Standard 1.2V 0.13µm CMOS", ISSCC Dig. Tech. Papers, pp. 524-525, 2007.

[2] L. Risbo and C. Neesgaard, "PWM Amplifier Control Loops with Minimum Aliasing Distortion", 120th Audio Engineering Society Convention, paper 6693, May 2006.

[3] T. Ido, S. Ishizuka, L. Risbo, F. Aoyagi, T. Hamasaki, "A Digital Input Controller for Audio Class-D Amplifiers with 100W 0.004% THD+N and 113dB DR", ISSCC Dig. Tech. Papers, pp. 1366-1367, 2006.