SAADC 10MS/s12b

Succesive approximation ADC

Features

- sample-rate up to 10 MS/s
- low power consumption, proportional to sample-rate:
  740 µW @ 10 MS/s
  7.4 µW @ 100 kS/s
- single-ended and differential mode
- 10.5 ENOB
- >80 dB SFDR (incl. THD)
- 0.15 mm^2 in baseline 0.18 µm CMOS
- rail-to-rail input range
- supports full Nyquist band
- silicon proven

Applications

- low-power applications
- sensor applications
- radio baseband processing

General description

This datasheet describes a general purpose Analog to Digital Converter (ADC) for low-power applications. The converter is a charge-redistribution successive-approximation type converter, suitable for the entire Nyquist band.

The key feature of this ADC is its low power consumption. This is achieved by using an energy efficient comparator and by making all circuitry dynamic. As a result, quiescent current in e.g. amplifiers is avoided, and the power consumption is fully proportional to the sample-rate. This property makes the ADC ideal for low duty-cycle sensor applications and other applications benefiting from low power consumption.

The converter can operate in both single-ended and differential mode, making it suitable for a broad range of applications.

The functional block diagram is shown in Figure 1.

The IP product described in this datasheet is silicon proven.

Block diagram

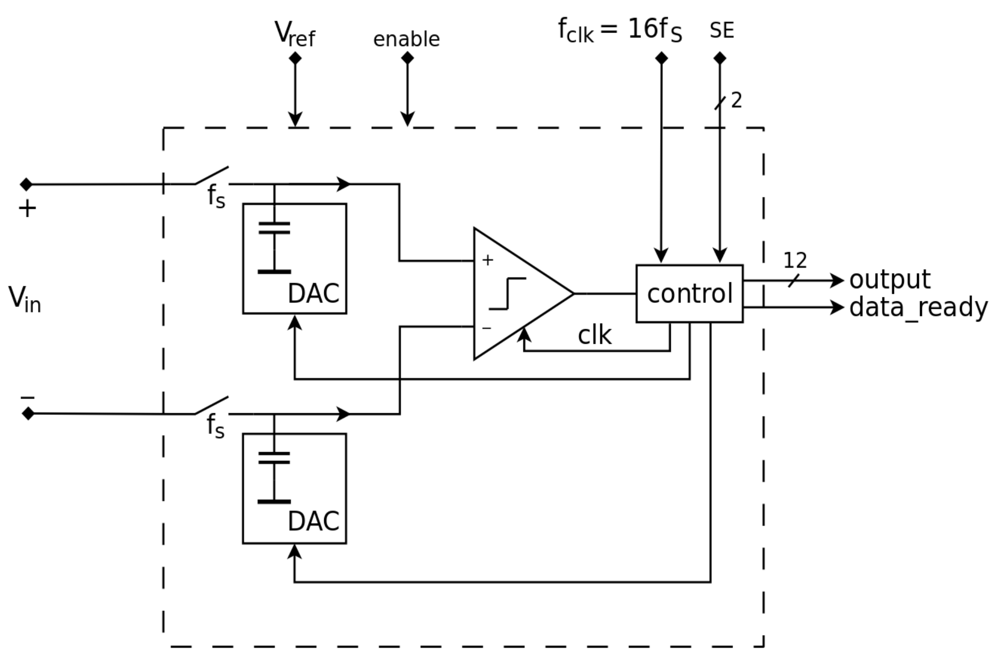

Figure 1: Block diagram of the Successive Approximation ADC

Specifications

Default test conditions

Supply voltage (V_{DD})	1.8 V
Reference voltage (V_{REF})	1.0 V
Clock frequency (f_{CLK})	160 MHz (ADC sample-rate: 10 MS/s)
Common-mode input voltage (V_{CM})	0.5 V
Temperature (T)	25 ºC

Electrical Specifications

Parameter	Description	Min	Typ	Max	Units
f_S	Sample-rate	0		10	MS/s
f_{CLK}	Clock frequency		16		f_S
V_{DD}	Supply voltage	1.65	1.8	1.95	V
V_{REF}	Reference voltage (without using reference buffer)	0.8	1	V_{DD}	V
V_{FS}	Full scale input voltage (single-ended)		0.95	1	V_{REF}
C_{IN}	Input capacitance (single-ended) This includes about 1 pF bondpad capacitance. If the ADC is integrated in a SoC this is reduced to about 0.2 pF.		2		pF
I_{IN}	Input current (single-ended) (e.g. 0.7 µA for a sample-rate of 10 MS/s)		0.07		µA / (MS/s)
P_{ADC}	Power consumption ADC at 100 kS/s (f_{IN} = 1.1 kHz) 10 MS/s (f_{IN} = 2.1 MHz)		 7.4 740		µW
P_{BUFFER}	Reference buffer [1)]		790		µW
Performance					
SFDR	Spurious Free Dynamic Range (f_{IN} = 2.1 MHz) (including harmonics)		80		dB
SNR	Signal to Noise Ratio (V_{IN} = 0 dB_{FS}, f_{IN} = 1.1 kHz)		66		dB
ENOB	Effective Number Of Bits (f_{IN} = 1.1 kHz)		10.5		bits
FoM	Figure of Merit defined as: $\frac{P}{2^{ENOB} \cdot f_S}$ (at both 10 MS/s and 100 kS/s)		0.05		pJ / conv. step
DNL	Differential Non-Linearity		± 1.5		LSB
INL	Integral Non-Linearity		± 2		LSB
Implementation					
Area	Die area in 0.18 µm CMOS		0.15		mm^2

Table 1: Specifications of the Analog-to-Digital Converter
Notes: 1) A reference buffer is included on the test chip, which is available as a separate IP block, see section Options.

Port list

Port name	Width	Description
GND	1	Ground
VDD	1	Supply voltage
VREF	1	Reference voltage, loaded with switched capacitor circuit
CLK	1	Clock signal at $16 \cdot f_S$
ENABLE	1	Enable signal for the converter (active high)
VINP	1	Non-inverting analog input signal
VINN	1	Inverting analog input signal
PSE	1	Selects VINN as single-ended input (active high). VINP must be connected to ground externally. If both PSE and NSE are low, VINP and VINN act as a differential input.
NSE	1	Selects VINP as single-ended input (active high). VINN must be connected to ground externally. When both PSE and NSE are low, VINP and VINN act as a differential input.
OUT	12	Digital output signal, non-inverting, unsigned binary
DATA_READY	1	Indicates that the conversion is complete and the output is updated. This signal can be used to re-clock the output data. (active high)

Table 2: port function description

Detailed description

The SE signals select which of the two inputs (V_{INP} or V_{INN}) is used as the single-ended input; the other input should be grounded. If both SE signals are zero, the converter operates in differential mode.

After the enable signal is made active high, the ADC will track the input signal at the next rising edge of clk, as indicated in Figure 2. At the next rising edge of clk, the input signal is sampled and the conversion is started. After finishing the conversion, the output code is updated and the data_ready signal is activated. This signal can be used to re-clock the output data.

The ADC core requires a clock frequency (f_{CLK}) of $16 \bullet f_S$ and a buffered reference voltage (V_{REF}) that is able to drive a switched capacitor network. The capacitance of this network is around 1 pF. This buffered voltage can either be made by an on-chip reference buffer, or it can be applied externally. In case V_{DD} is sufficiently clean, it can also be used as the buffered reference voltage. The reference voltage determines the full-scale voltage of the ADC.

Basically, the input impedance is purely capacitive, since at the end of the conversion, the charge on the capacitors is restored before the sample-switches are re-activated. Due to parasitic capacitance a small DC current (proportional to the sample frequency) will flow into the input nodes.

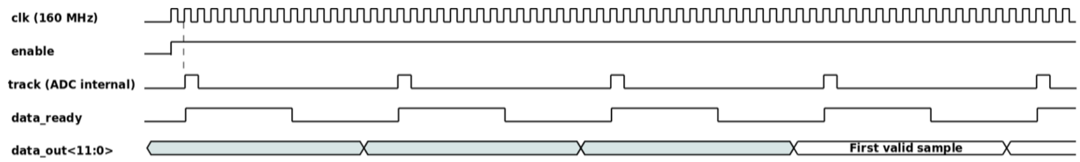

Figure 2: Timing diagram of the ADC

Deliverables

The IP deliverables consist of a GDS file, a behavioral model, a netlist and integration documentation. The product can be delivered as a single IP component for customer integration or Axiom IC engineers can integrate the product as part of a SoC engagement.

Options

For generating the buffered reference voltage, Axiom IC offers energy-efficient reference buffers specifically aimed at this converter and adjustable to the customer's requirements.

The converter can also be extended with gain and/or offset calibration.

For more information about these options, please contact us at info.enschede@teledyne.com.

Revision history

The following table lists the revision history, only major revisions are shown.

Revision	Date	Reason for revision
F9	2017-07-18	Template update
F8	2014-08-29	Clarified polarity of inputs w.r.t. PSE/NSE signals
F7	2012-03-22	Expanded descriptions of V_{IN}, SE and Enable signals. Updated detailed description and added timing diagram. Updated specs C_{IN}, V_{FS} and SFDR. Added Nyquist operation band.
F4	2010-09-17	Included description and values about input current

Table 3: Document revision history

For more information about Teledyne DALSA
visit our Web Site at

http://www.teledynedalsa.com/semi/mixed-signal/

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