AXIOM_LLSDADC100dB

High Resolution Low Latency ΣΔ ADC

Features

- High dynamic range: >100dBA (20Hz – 20kHz)
- Low power: 1.6mW per ADC
- Low Area: 0.3mm^2 per ADC
- Low latency: only one clock period (40ns)
- Low noise reference without external components
- Supports wide common mode range
  (true ground to supply & capacitive coupling)
- Supports both differential and single-ended input
- Supports 4 internal gain settings
- Using external resistors allows:
  - Additional gain settings
  - Extended input voltage range, well outside supply voltage range
- Silicon proven in 0.14µm CMOS

Applications

- High-quality audio ADC & DAC (codec)
- Digital control loops (enabled by its low latency)
  - Digital (Class-D) Amplifier
  - Noise cancellation
- Sensor read-out
- Instrumentation

Description

The AXIOM_LLSDADC100dB is a low power variant of our high-resolution sigma-delta analog-to-digital converter family. It achieves a dynamic range of more than 100dB, at a power consumption of only 1.6mW.

The latency of the ADC is only one clock cycle (40ns at 25MHz), which makes the converter ideally suited for application in control loops. The low latency is enabled by feeding the bitstream output back to the input via a DAC with build-in filtering. This creates a “tracking ADC behavior”, where the output accurately tracks the input signal inside the signal bandwidth. Next to enabling low latency, the filtering DAC also makes the system robust towards jitter and other error sources typically associated with 1-bit converters.

The AXIOM_LLSDADC100dB can convert both single-ended and differential signals with high accuracy. Next to this it can convert signals with amplitudes and biasing levels well outside its own supply level, by using external resistors acting as level shifters.

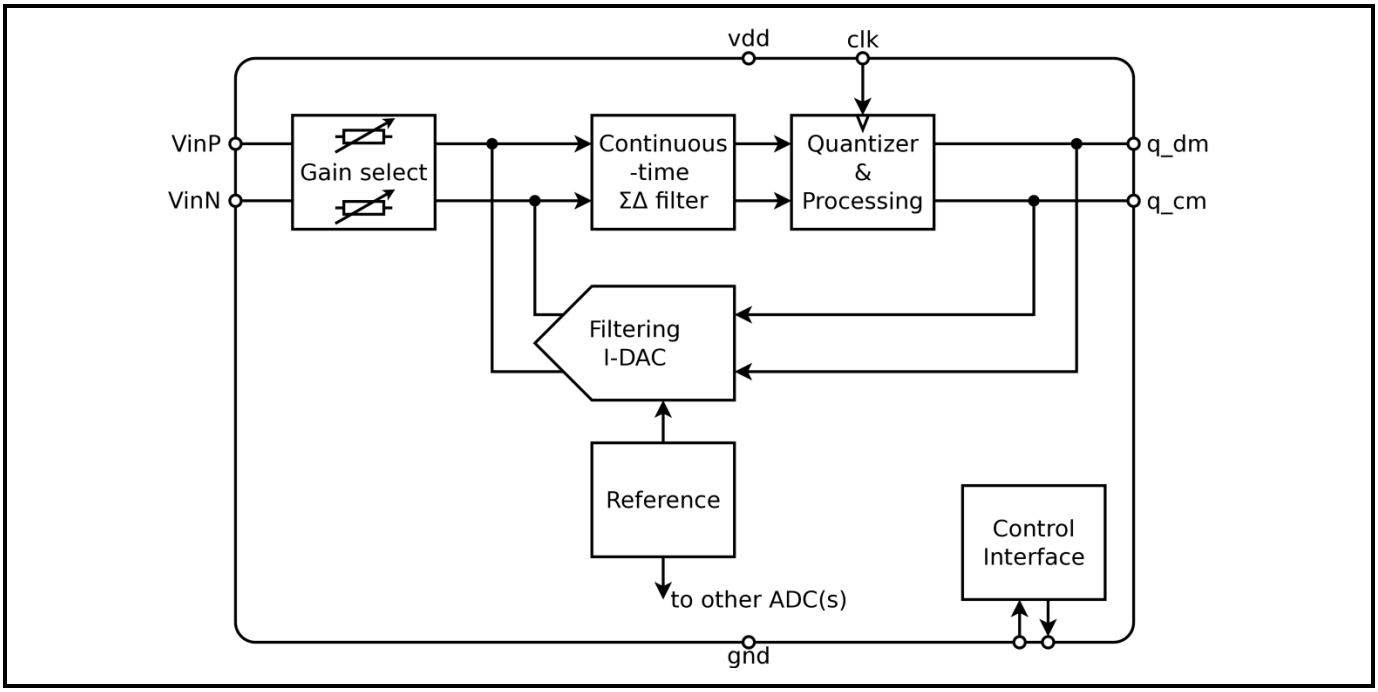

Figure 1 – Block diagram of the AXIOM_LLSDADC100dB.

Specifications

Default test conditions

Supply voltage (V_{DD}) 1.8 V
Input clock frequency (f_{CLK}) 24.576 MHz
Audio sample rate (f_S) 48 kHz
Temperature (T) 25 °C

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
TECHNOLOGY					
Process	0.14µm CMOS technology		0.14		µm
Area ADC	Area of one ADC		0.3		mm^2
Area Refgen	Area of reference generator		0.2		mm^2
TEMPERATURE					
T_{OP}	Functional operating temperature	-40	25	125	ºC
ELECTRICAL					
V_{DD}	Analog supply voltage	1.65	1.8	1.95	V
V_{REF}	Internal reference voltage		0.9		V
V_{CM}	Common-mode input voltage		0.9		V
I_{DD_ADC}	Supply current per ADC		0.9		mA
I_{DD_REF}	Supply current of reference		0.9		mA
R_{IN}	Differential input resistance of ADC (per gain setting)		20.0 (0dB) 14.1 (+3dB) 10.0 (+6dB) 7.1 (+9dB)		kΩ
f_S	Supported audio sample rates	32		48	kHz
f_{CLK}	Input clock frequency		512 × f_S		Hz
PERFORMANCE					
DR	Dynamic Range[1]	100	102		dBA
V_{FS}	Full scale differential input voltage (per gain setting)		1.00 (0dB) 0.71 (+3dB) 0.50 (+6dB) 0.35 (+9dB)		Vrms
I_{FS}	Full scale input current		50		µArms
OUT_{FS}	Output code at full-scale input[2]		-3		dBFS
$SINAD_{FS}$	Signal to Noise And Distortion ratio at full scale input		70		dB
$SINAD_{MAX}$	Maximal obtained SINAD (Figure 6)		87		dB
THD	Total Harmonic Distortion at 3dB below full scale input		-91		dB
IM	Intermodulation products[3]		-92		dB
PSR	Power Supply Rejection[4]		90		dB
CM2DM	Common-Mode to Differential-Mode conversion		-40		dB

Table 1 – Specifications of the AXIOM_LLSDADC100dB

[1] Test condition: SNR measurement (20-20 kHz) @ 60 dB below full scale input; DR = SNR+60 dB, A-weighted.
[2] Output code for a single-tone input wrt. full-scale digital output (0 dBFS: the max. representable digital sine wave).
[3] Test condition: 2-tones at 19.5k and 20.5 kHz, both at 6 dB below full scale input.
Measured is the highest IM-product w.r.t. to level of one of the input tones, see Figure 5.
[4] Test condition: 100 mVpp / 217 Hz sine wave on supply; delta of PSR spur w.r.t. full-scale digital output (0 dBFS).

Measured Performance

The following measurements are performed using an Audio Precision APx 525 with a PDM module. Full bitstream is captured at PDM input, decimation is done by the APx 525.

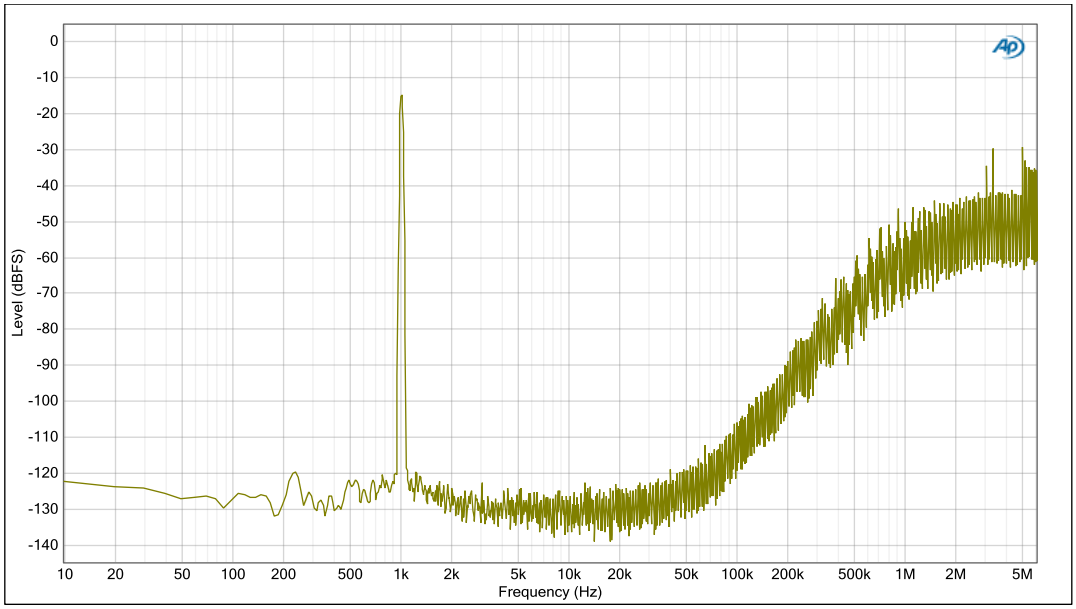

Figure 2 – Wideband output spectrum of a 1kHz, 0.25V_{RMS} input signal in 0dB gain-mode.

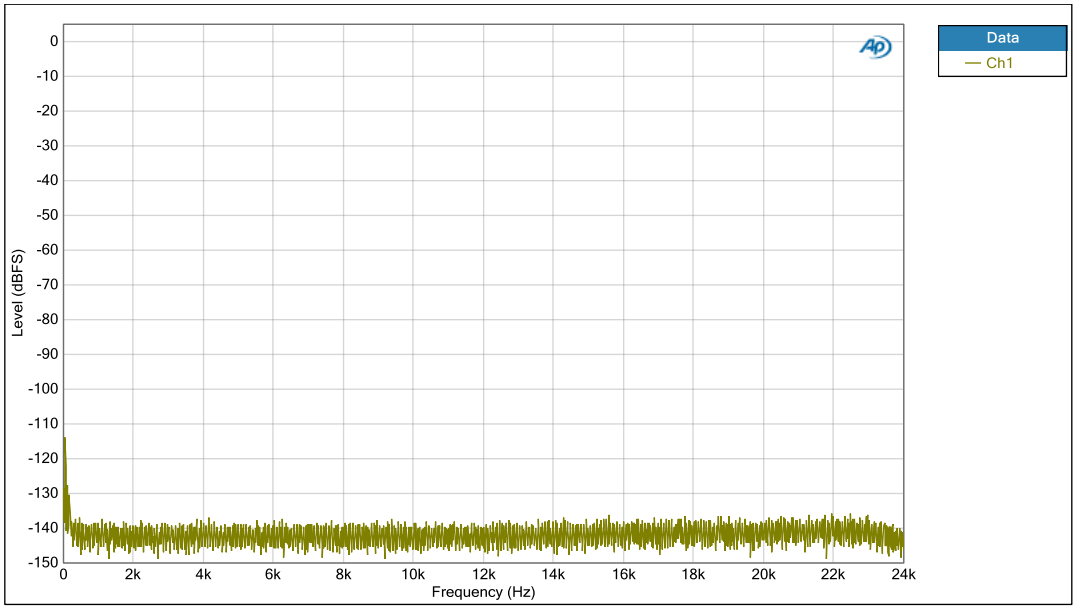

Figure 3 – Noise floor of a 256x decimated output.

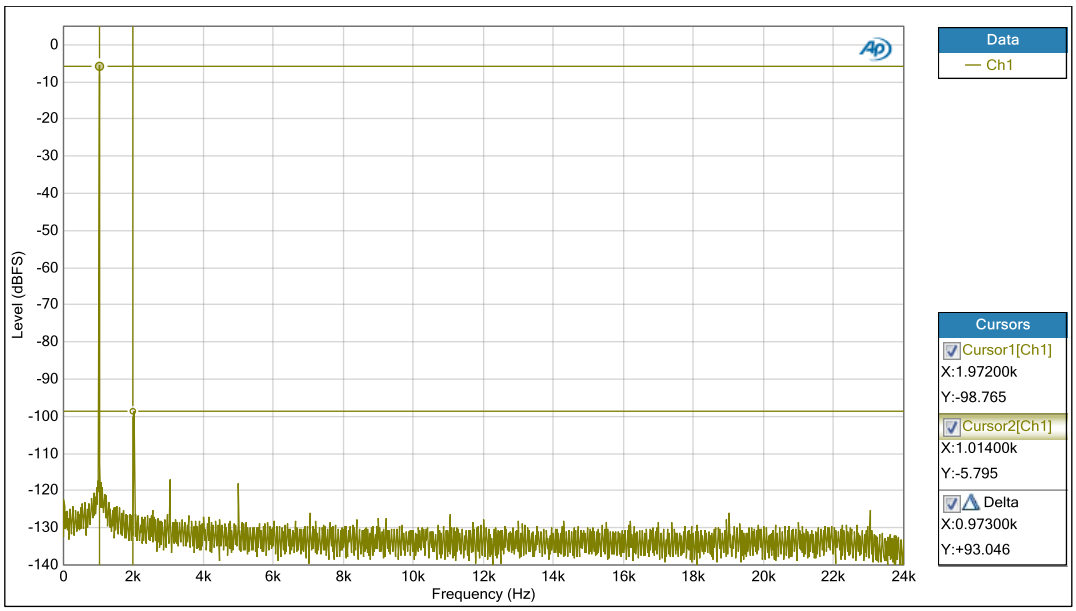

Figure 4 – Audio band output spectrum (256x decimated) of a 1kHz, 0.7V_{RMS} input signal in 0dB gain-mode.

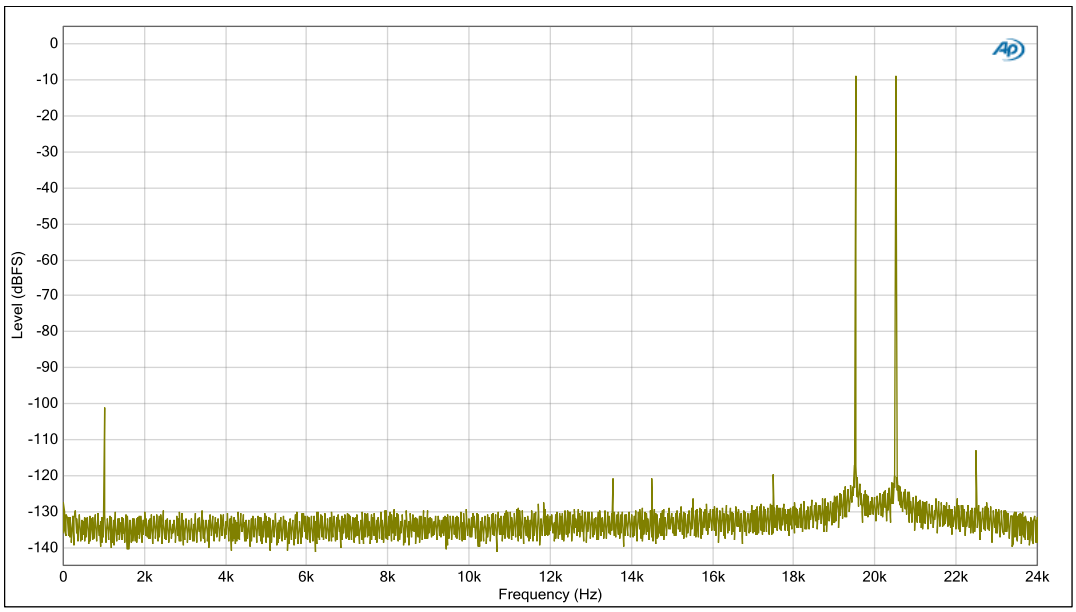

Figure 5 – Intermodulation spectrum of a 19.5k and a 20.5kHz tone, both at 6dB below full-scale input.

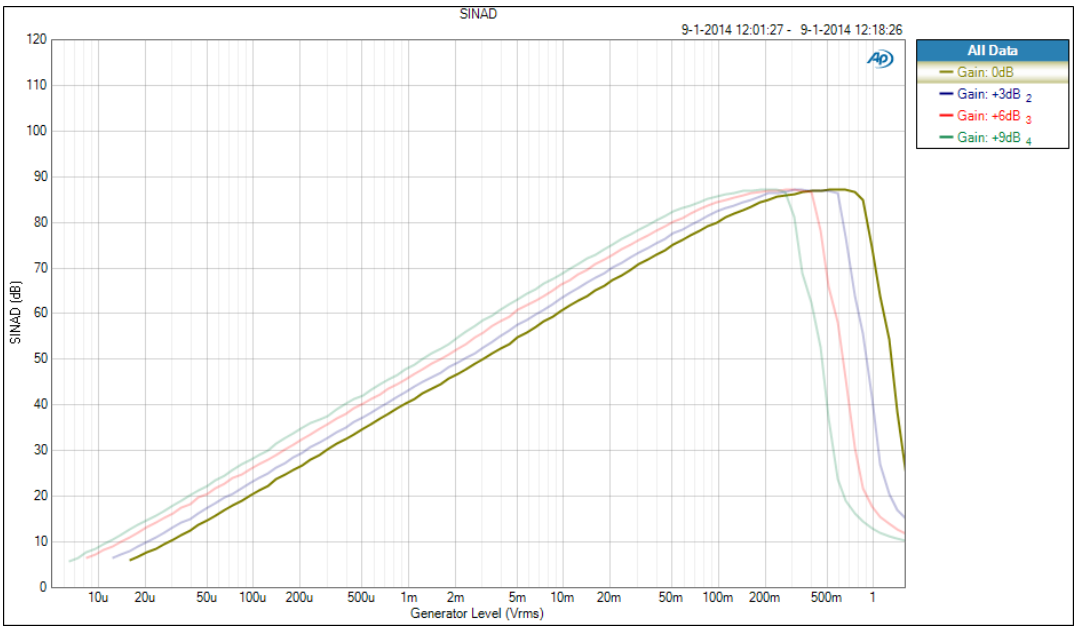

Figure 6 – SINAD (20-20kHz, unweighted) vs. input signal, for the 4 gain-settings.

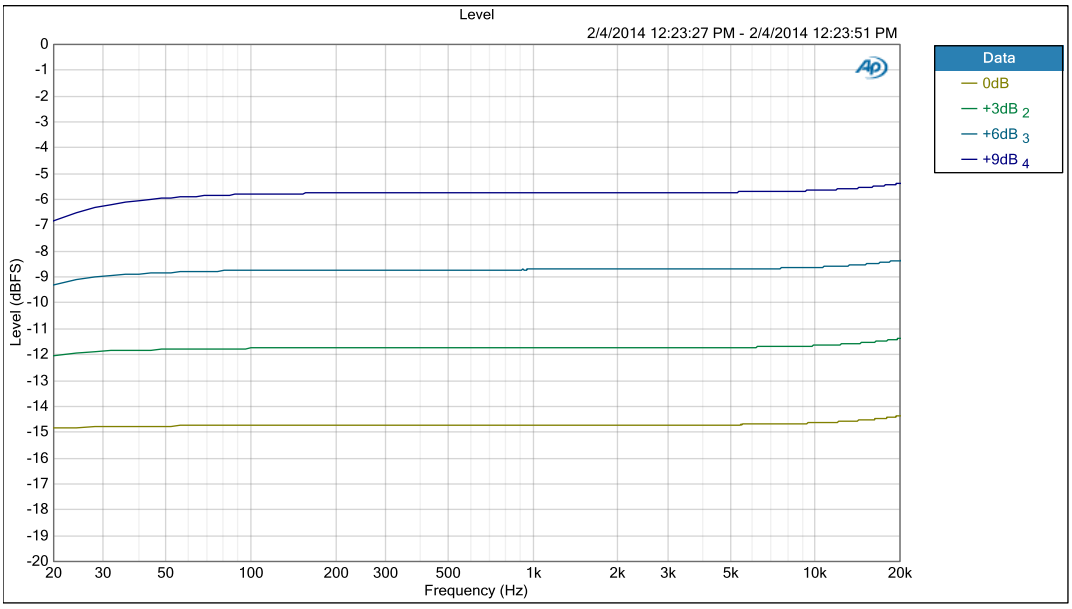

Figure 7 – Output level vs. frequency (20-20kHz) at 0.25V_{RMS} input signal amplitude, for the 4 gain modes.

Note: The decrease of output level at low frequencies, for higher gain settings, is caused by the external AC-coupling capacitors used for this measurement.

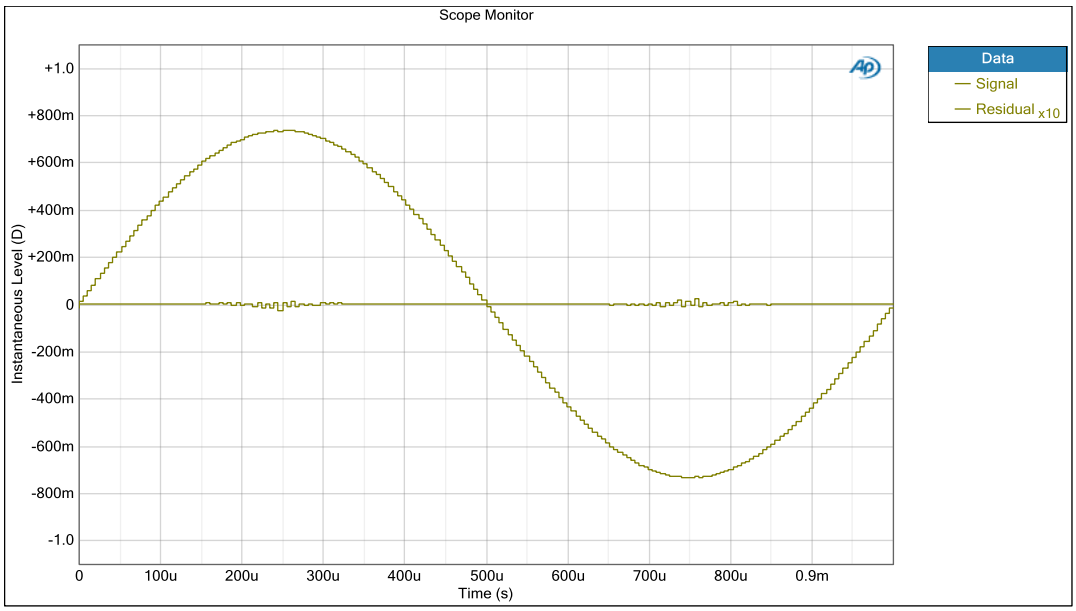

Figure 8 – Output signal (64x decimated) vs. time of a 1kHz, $1V_{RMS}$ in 0dB gain-mode (full-scale input).

Note: The residual signal, the deviation of the output signal from a perfect sinusoidal, is shown in Figure 8 (amplified 10x). The error w.r.t. a perfect sinusoidal signal is still small at full-scale input.

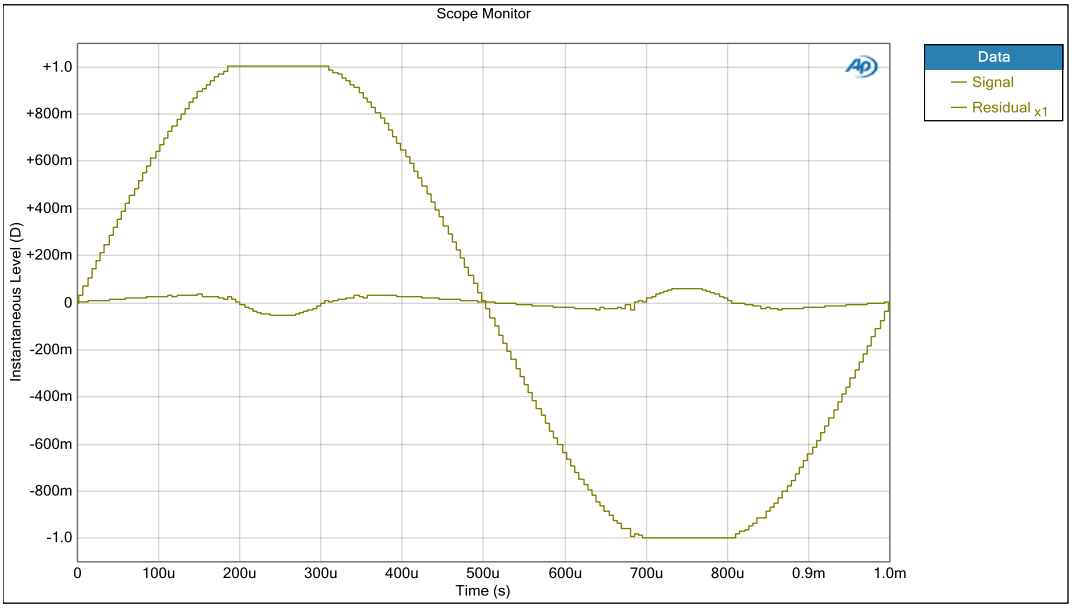

Figure 9 – Clipping signal (64x decimated) of a 1kHz, $1.5V_{RMS}$ in 0dB gain-mode

Note: The ADC has nearly ideal clipping behavior, no sticky-clipping or other clipping artefacts are observed.

Applications

The AXIOM_LLSDADC100dB is versatile and can be used in many applications; examples of applications are given in the following sections.

Digital noise cancellation

The AXIOM_LLSDADC100dB is well suited to digitize the output of a microphone. The latency of the AXIOM_LLSDADC100dB (~40ns) is more than 1000 times lower than the period of a 20kHz signal (50us). This unique property of the AXIOM_LLSDADC100dB enables truly digital noise cancellation with feedback, using adaptive noise suppression algorithms. The application diagram is shown in Figure 10. The digital noise cancellation core combines the unwanted noise signal (sensed via mic) with the wanted signal (in) such that at the output the unwanted signal is suppressed at the speaker/headphone.

Instrumentation

The AXIOM_LLSDADC100dB can be used to make precision measurements for a wide range of input configurations. Figure 11 shows three input configurations, fully differential, single-ended and true ground. Both the differential and the common-mode signal are converted to a bit stream and available at the output. In the AXIOM_LLSDADC100dB the conversion resistors are integrated on-chip. Alternatively, the AXIOM_LLSDADC100dB can operate with external resistors to extend the differential and common input range to levels well outside its supply voltage range.

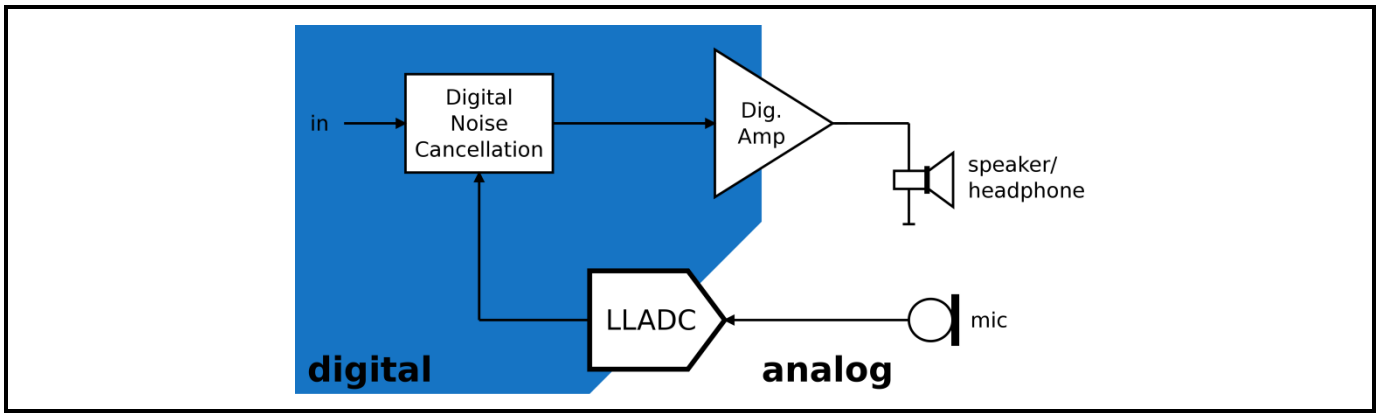

Figure 10 – Application of the AXIOM_LLSDADC100dB (“LLADC”) for digital noise cancellation.

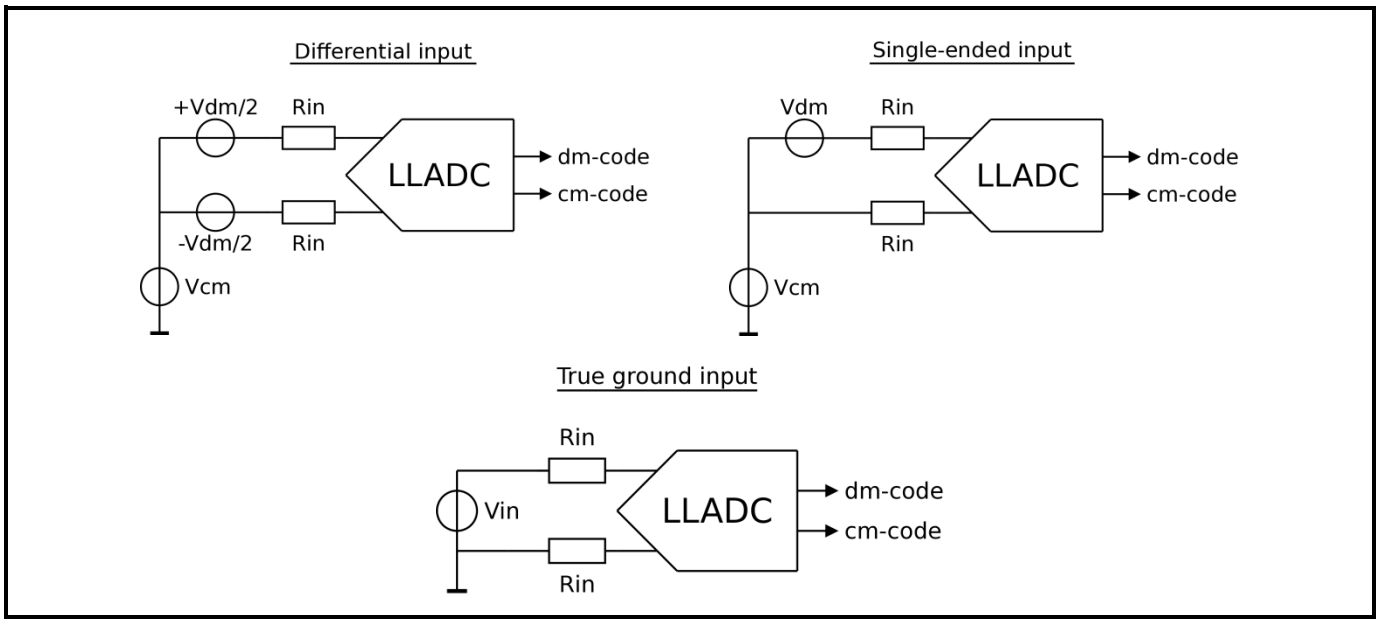

Figure 11 – Input configurations of the AXIOM_LLSDADC100dB for precision instrumentation measurements.

Digital amplifier

Enabled by its low latency, the AXIOM_LLSDADC100dB can be integrated in a truly digital amplifier. Figure 12 shows for example the embedding of the AXIOM_LLSDADC100dB in a Class-D amplifier with feedback after the LC-filter. The key advantages of a truly digital amplifier are: Improved performance due to digital loop design, fast design cycles and reduces costs. For more information on digital amplifiers see our 120 dB version at our website: http://www.teledynedalsa.com/semi/mixed-signal/HRLLSDADC/ (under applications you can find a presentation on the digital amplifier concept)

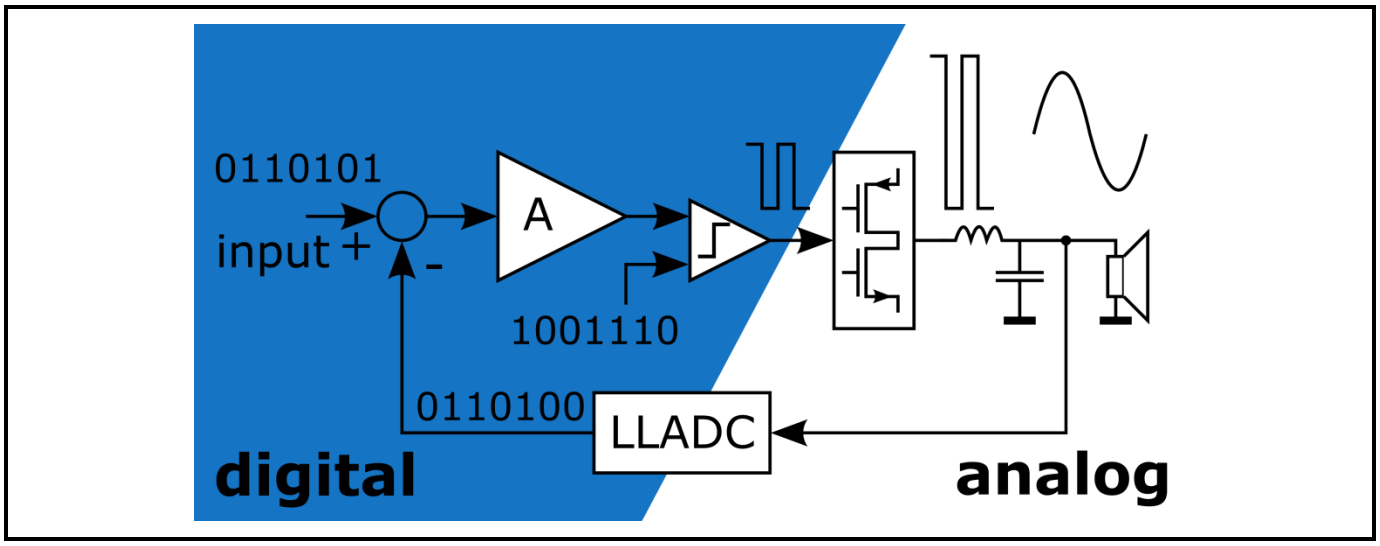

Figure 12 – The AXIOM_LLSDADC100dB (“LLADC”) embedded in a truly digital Class-D amplifier.

Delivery

The IP deliverables consist of a GDS file, a behavioral model, a netlist, a datasheet and integration documentation. The product can be delivered as a single IP component for customer integration or Teledyne Axiom IC engineers can integrate the product as part of a SoC engagement.

VIEW	FILE TYPE	DESCRIPTION
Behavioral model	VHDL / Verilog / Simulink	Behavioral model of the IP which can be used for simulation purposes
Netlist	CDL	Netlist for LVS checks
Layout	GDS2	Layout database
Abstract	LEF	Abstract view with layout boundaries and pinning information
Checks	DRC/LVS/ANT	Verification checks results performed on the layout
RTL	VHDL	VHDL code
Module header	INTERFACE	VHDL module header
Timing & interface	SDC & LIB	Timing constrains and interface information
Design documentation	PDF	Datasheet, specifications and simulation results
Integration documentation	PDF	Interface description for integration

Table 2 – Deliverables of the IP

Revision history

REVISON	DATE	REASON FOR REVISION
F5	2014-03-03	Version for publication on the website, corrected references to figures and typos

Table 3 – Document revision history

For more information about Teledyne Axiom IC visit our Web Site at

http://www.teledynedalsa.com/semi/mixed-signal/

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