FAIR, a front-end ASIC for infrared detector readout

J.H.R. Schrader[a] , K. Garakoui[b], D. Schinkel[b]

[a]SRON Netherlands Institute for Space Research, 3584CA Utrecht, The Netherlands
[b]Axiom IC Teledyne Dalsa, 7521 PT Enschede, The Netherlands

j.h.r.schrader@sron.nl

Abstract

In the FAIR project (Front-end ASIC for Infrared detector Readout), an IC is developed for the readout of state-of-the-art NIR/SWIR detectors for future Earth observation missions and astrophysics. The chip consists of a high-resolution ADC with integrated offset correction and adjustable gain, and voltage regulators to generate bias/reference voltages for the detector.

The ADC has a 16-bit resolution and offers a sampling rate of 1 Megasample per second. It is designed for an ultra-low power consumption of 16mW. The ADC analog circuitry area is 2mm^2 in 0.18µm CMOS.

The chip is designed to operate in a large temperature range from -218 degrees Celcius up to 50 degrees Celsius, because the original mission goal was for the Exoplanet Characterization Observatory (EChO). The close proximity to the cooled detector requires the read-out electronics to operate at an equally reduced temperature. Considering that the target atmospheric gases addressed by EChO - CH_4, CO, CO_2 and H_2O - are the same as addressed by current and future in Earth-observation missions in the SWIR-IR spectral range (e.g. ESA CarbonSat, CNES MicroCarb), it is clear that the FAIR chip also offers interesting opportunities for application in future Earth observation missions.

The FAIR chip can be placed naturally into the existing electronic readout environment for application to other future IR detectors, replacing and significantly miniaturizing the analog electronics, fitting in the on-going trend of integration in detector electronics for space instrumentation in general: obvious advantages are the reduction of power consumption, volume and weight.

Special analog layout techniques were used to ensure radiation hardness, and all digital circuitry was place&routed using the rad-hard IMEC DARE library.

I. Introduction

There are several upcoming Earth-observation missions that have cooled IR detectors as their baseline, e.g. ESA's Carbonsat, and the French MicroCarb instrument. An ASIC based design for the front-end significantly reduces the budgets on mass, volume, and power, and allows for more flexibility in the board design and integration. Furthermore, it allows the front-end electronics to be placed as close to the (cooled) detector as possible. The analog signals from the detector need only travel a short distance to the ASIC, where they are amplified and digitized. The signal integrity and immunity to electromagnetic interference (EMI) is thus improved. Furthermore the entire front-end IC can be qualified for low temperature operation in one single test campaign.

A typical IR detector front-end readout circuit consists of the following blocks:

1. low-noise high-stability pre-amplifiers with gain and offset compensation
2. analog-to-digital converters (ADCs)
3. power regulators, bias, reference voltage generators
4. housekeeping (voltage / current monitoring)
5. digital clocking and pixel addressing.

As a first step toward a fully integrated front-end chip, we started by integrating the parts most critical for signal integrity: the amplification and digitization of the detector signals. The chip block diagram is shown in Fig. 1. This 'heart' is formed by four independent signal processing chains (to match the four analog pixel outputs of the detector). The chip comprises of a low-noise pre-amplifier functionality with gain and offset compensation and of analog-to-digital converters (ADCs). Furthermore, voltage regulators are included for controlling the IR detector bias & reference voltages.

Pixel clocking, addressing, and configuration functionality is vendor specific. We chose to leave this out of the ASIC. It can be placed in an external FPGA to offer the greatest flexibility and widest applicability to detector chips from different vendors.

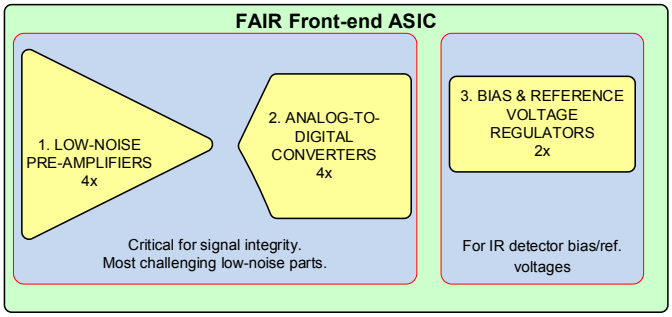

Fig. 1. Block diagram of FAIR front-end ASIC

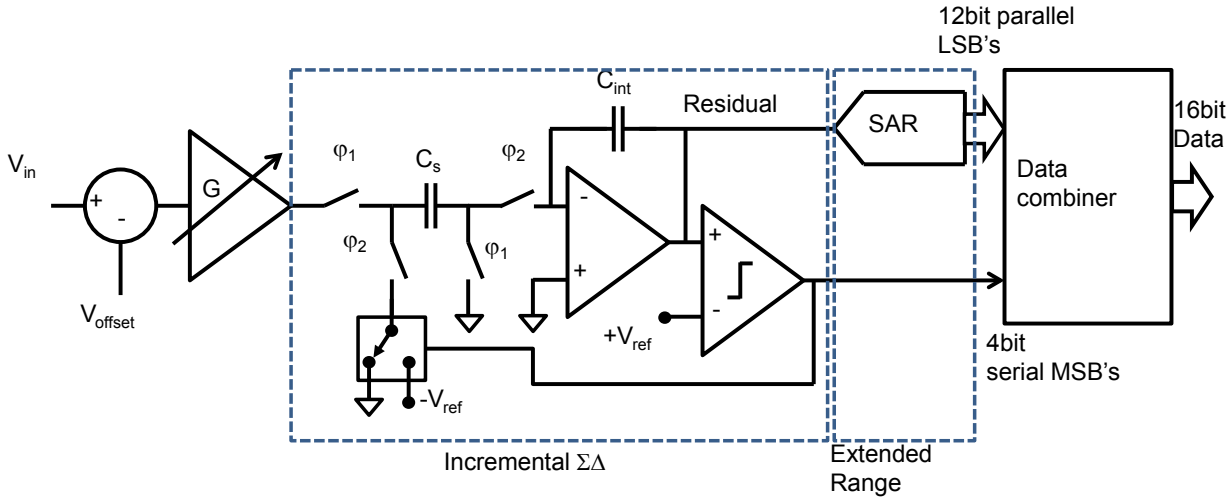

Fig. 2. Architecture of analog signal processing chain.

II. Chip Specifications

The FAIR chip specifications are given in Table 1.

Technology	UMC 0.18um CMOS
Supply voltage	3.3V (analog) 1.8V (digital)
Operating temperature range	40K - 328K
Analog front-end	
No. of independent front-end chains	4
Gain settings	1x, 2x, 4x 8x
Offset compensation range	0.5..3V
Offset DAC resolution	24 bits
Analog input voltage range	0V..3V
Analog input capacitance	12-16pF
Analog-to-digital converters (ADC)	
ADC sampling frequency	1.0 MHz
Analog bandwidth	500kHz
Resolution	16 bits
Effective number of bits (target)	15 ENOBs
Bias and reference voltage generators	
No. of independent regulators	2
Output bias/ref voltage range	0 .. 2.8V
DAC resolution	24 bits
Max current	2mA

III. ADC Architecture

The analog front-end is the heart of the ASIC and its quality is critical to the signal integrity. Our prime focus was therefore on the pre-amplifier and the analog to digital conversion (ADC) for the pixel signals.

The requirements for the ADC are quite stringent. The low noise and low distortion requirements in combination with the sample-rate require a very high-performance ADC. Normally, one would use sigma-delta type of ADC for this purpose, as sigma-deltas can combine high resolution with high sample-rates. (Classical algorithms to obtain high resolution, such as dual-slope converters, operate at much lower sample-rates.) However, a normal sigma-delta converter works under the assumption that the sampled signal is a single band-limited signal and not a multiplexed signal. For a normal sigma-delta to work with a multiplexed signal, the states have to be stored between every signal switch which is not very practical.

To circumvent this problem, a special type of sigma-delta converter has emerged in recent history, which is suitable to convert multiplexed signals, the so-called 'incremental ADC'. For more background information on this type of ADC, see e.g. [1]. A drawback is that incremental sigma-delta ADCs require quite many clock-cycles to reach a high resolution. For example about 400 clock cycles are required per sample when a second-order sigma delta would be used to reach the required 16-bits of resolution [1]. This is much more than the 16 cycles that are required for a classical binary search algorithm. However, converters that typically use search algorithms such as successive approximation (SAR), pipeline or algorithmic ADCs, are not natively suitable to obtain high resolutions (unless very complex calibration algorithms are used).

The architecture of the analog front-end is shown in Fig. 2. To obtain the best of both worlds and combine high resolution with a low number of clock-cycles per sample, a hybrid converters is used. An example of such a converter is given in [2], were an incremental ADC is combined with a successive approximation ADC, with the latter extending the range of the former. In this publication a resolution of almost 16bits (90.1dB) is achieved over a bandwidth of 1MSample/s, with a clock-frequency of only 45MHz (45 cycles per sample).

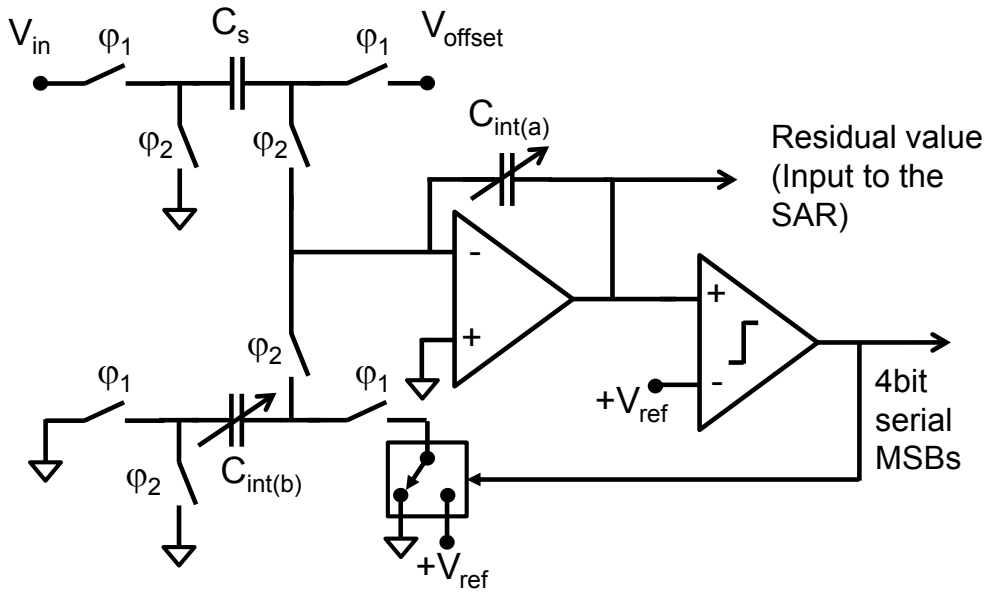

Fig. 3. Incremental sigma-delta front-end circuit with gain and offset cancellation

Such a hybrid converter is also best suitable for this application. The remaining challenge in this project was to further reduce the noise-floor to more than 16 bits and create a system that is radiation hard and can operate at low temperature.

A. ADC front-end with offset compensation and adjustable gain

Implementation of the offset cancellation circuit and the variable gain preamplifier for the ADC in a traditional way would require extra active circuits. An offset compensation mechanism is required because the base level of the IR detector output is around 1.0V (no light). An adjustable gain is needed to be able to use the full ADC resolution under any light conditions. Two extra opamps (beside the opamp used for implementing the integration function) would be needed for the mentioned purposes. The existence of these circuits at the front of the ADC would add extra noise and nonlinearity to the input signal. Therefore they would need to be designed quite linearly and would need to consume enough power to satisfy the low noise requirements of the 16bit conversion. The power consumption limitations required a new circuit topology to satisfy all functions with the lowest possible number of active circuits. Therefore, a new circuit topology has been introduced which merges offset cancellation, gain and integration functions into a single circuit.

In Fig. 3, the front-end circuit is shown. During phase φ_1, V_{in}-V_{offset} is sampled at capacitor C_s and during phase φ_2, the sampled value is integrated on $C_{int(a)}$. At each period the output voltage of the integrator (residual value) is compared to a fixed reference voltage ($+V_{ref}$), and in case of exceeding a fixed amount of charge is subtracted from C_{int}(a). The subtraction action is done via charging $C_{int(b)}$ to the ($+V_{ref}$) voltage. The tunable capacitors $C_{int(a)}$ and $C_{int(b)}$ are equal to each other. The pre-amplification factor for the total circuit is controlled by changing the ratio between C_s and $C_{int(a)}$. A 0-20dB controllable gain with a 3dB step size was implemented by this technique. After 16 cycles of integration in the incremental sigma delta converter, 4 serial bits come out and also a residual value comes out. The residual value is fed to the SAR to produce the rest of the 12 bits. The total operation is called "Extended range incremental sigma delta converter" and results in a 16 bit resolution. No ADC range is lost due to the offset voltage compensation mechanism.

B. Low-temperature operation

The low temperature operation at 55 Kelvin gives two effects on the CMOS transistors:

1) higher threshold voltages for the CMOS transistors

2) higher carrier motilities (low scattering).

At 55 Kelvin, compared to operation at the room temperature (27°C), transistor transconductance will be higher for the same current consumption. The g_m of each single transistor changes with 1dB in this range. Therefore in this large operating temperature range, gain of the opamps can vary and cause instability. Therefore large phase and gain margins for the integrators were taken to satisfy the operation of the system both at room temperature and 55 Kelvin temperature.

IV. BIAS / REFERENCE VOLTAGE REGULATORS

The bias / reference voltage regulators have a PMOSt common source output stage, and the feedback resistors are used as a load (therefore an NMOSt current source is not

needed). The opamps in the regulators have a PMOSt input pair. In Fix 4, the circuit diagram is shown.

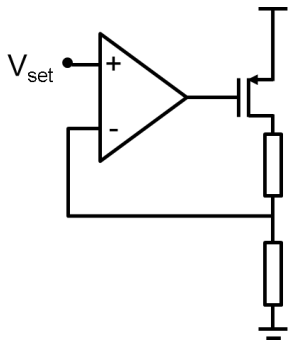

Fig.4. Bias / reference voltage regulator circuit

V. Chip design

The GDS of the complete design is shown in figure 5. This is the end version as submitted to the fab. On top, there are 4 ADCs. On the bottom, from left to right: the bias/ref. voltage regulators (small block), and 3x the DACs (large blocks). One DAC generates the offset voltage as an input to the ADCs, and the other two are for the bias/ref. regulator control. The dark blue space between the blocks is filled with rad-hard cells from the DARE library (sea-of-gates).

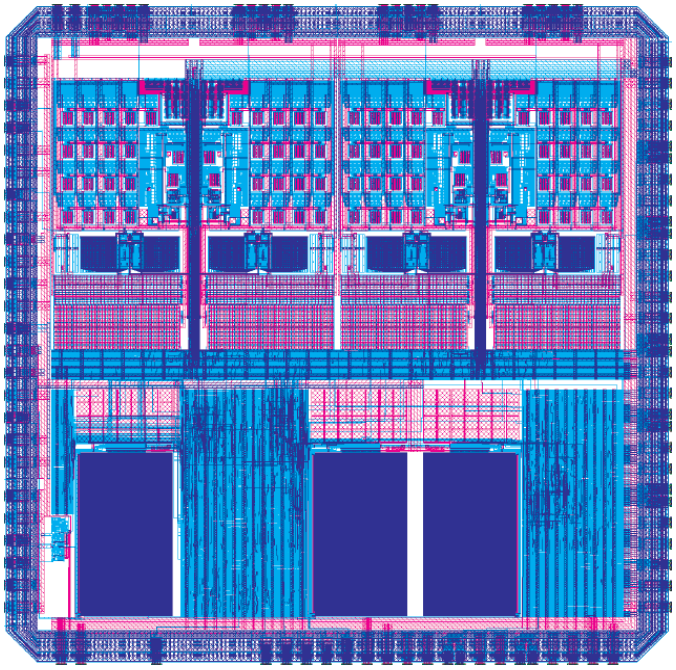

Fig. 5. GDS view of the complete design

VI. Planning

The packaged chip will be back from processing in July, and then we will start measurements.

VII. Conclusion

An IC for the readout of state-of-the-art NIR/SWIR detectors for future Earth observation missions and astrophysics was presented. The 16 bit, 1 Megasample/s, 16mW ADC with hybrid sigma-delta/SAR architecture offers integrated offset correction and adjustable gain. The ADC analog circuitry area is $2mm^2$ in 0.18µm CMOS. Voltage regulators are included on the chip to generate bias/reference voltages for the detector. The chip is designed to operate in a large temperature range from -218 degrees Celcius up to 50 degrees Celsius. Testing will start in July 2014.

VIII. References

[1] Markus, J.; Silva, J.; Temes, G.C., "Theory and applications of incremental ΔΣ converters," Circuits and Systems I: Regular Papers, IEEE Transactions on , vol.51, no.4, pp. 678- 690, April 2004.

[2] Agah, A.; Vleugels, K.; Griffin, P.B.; Ronaghi, M.; Plummer, J.D.; Wooley, B.A. , "A High-Resolution Low-Power Incremental ΣΔ ADC With Extended Range for Biosensor Arrays," Solid-State Circuits, IEEE Journal of , vol.45, no.6, pp.1099-1110, June 2010.