Very-low Dark Current in FF-CCDs

I. M. Peters, E. W. Bogaart, W. Hoekstra, A. C. M. Kleimann and J. T. Bosiers

DALSA Professional Imaging,
High Tech Campus 27, 5656 AE Eindhoven, The Netherlands
inge.peters@dalsa.com - phone +31-40 259 9066 – fax +31-40 – 259 9005

Abstract

We achieved a dark current of 1.5 pA/cm^2 at 60 ºC for a Full-Frame CCD with 6x6 μm^2 pixel size without compromising good charge handling capacity, vertical anti-blooming, and electronic shuttering. In this paper, trade-offs in the pixel design will be discussed and results on sensor and dark current performance will be presented. [1]

Introduction

In low-light level conditions, low dark current essential to capture good images. Since the largest contribution of dark current is generated by the interface states, the reduction of dark current is achieved by creating a hole layer at the entire Si-SiO_2 interface, known as multi-pinned phase (MPP) [1,2], This approach is often used in full-frame CCDs with large pixel sizes (12x12 μm^2 or larger). Since this MPP concept does not support anti-blooming and electronic shuttering, this limits the application to specific areas of scientific imaging.
We have previously reported on our 'all-gates-pinning' (AGP) concept that combines MPP with both vertical anti-blooming and electronic shuttering for 6.9x12.6 μm^2 [3] and 9x9 μm^2 pixels [4]. We have further improved this concept in the 6x6 μm^2 pixel design intended primarily for use in professional digital still photography.

Development of improved AGP pixel

In figure 1, a schematic overview of the pixel is given. AGP requires an additional n-implant below 2 of the 4 image gates compared to the standard 6x6 μm^2 pixel design. In addition, the p-implant is slightly changed, so that only 2 different masks are required for introduction of AGP in our standard 6x6 μm^2 sensor [5]. Extensive simulations have been done to find the optimum implant dopes and conditions. Trade-offs had to be made between charge handling capacity on one hand and the pulse height required for electronic shuttering on the other hand. Two different n-implant configurations have been investigated; DN1-DN2 is 1.0-1.0 and 1.0-1.3.

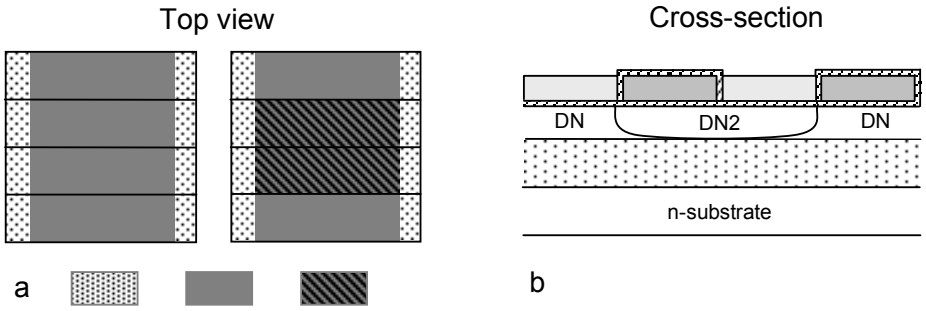

Figure 1
a) *Top view of n-channel implant (DN) for conventional pixel (left) and extra n-channel implant (DN2) for AGP pixel (right). SP = channel stop implant*
b) *Cross section along transport direction of AGP pixel. DN is the first n-channel implant and DN2 is the second n-channel implant (non self-aligned).*

[1] Part of this work is submitted to 2009 special issue of IEEE Trans. on Electron Devices.
This work was supported by MEDEA+, Project 2A206 ASIC-CCD

The resulting potential profiles in the pixel, under the center of the integrating and blocking gates of figure 1, is shown in figure 2.

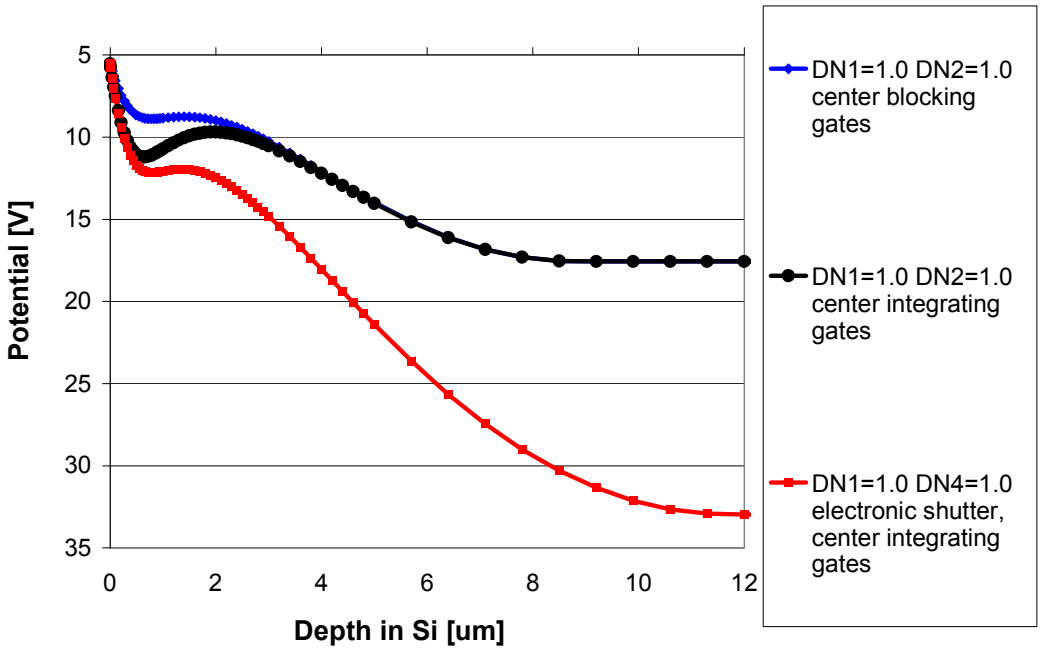

Figure 2. Potential profiles in AGP pixel

Evaluation Results

In table 1, an overview is given of the sensor performance for the two different n-implant combinations compared to the previously presented 9x9 µm^2 pixel results. All solutions have excellent performance on transport efficiency, quantum efficiency and vertical anti-blooming comparable to non-AGP sensors. The dark current for the 6x6 µm^2 pixel is improved with a factor of 2 compared to the 9x9 µm^2 pixel. As expected the 6x6 µm^2 AGP pixel with the higher charge handling capacity and thus a 'deeper' potential well also requires a larger pulse for electronic shuttering.

Parameter	**6x6 µm^2 DN1-DN2= 1.0 – 1.0**	**6x6 µm^2 DN1-DN2= 1.0 – 1.3**	**9x9 µm^2 [4]**
Qmax (ke$^-$)	17	30	50
Vertical transport efficiency	> 0.999 995	> 0.999 995	> 0.999 995
Quantum efficiency			
@ 460 nm (%)	19	19	18
@ 530 nm (%)	29	30	24
@ 590 nm (%)	31	33	24
Electronic shutter pulse (V)	19	>20[1]	10
Dark current at 60 ºC			
(pA/cm^2)	1.5	1.7	3
(e$^-$/s/pixel)	3.4	3.8	16

[1] 20V is current hardware limit

Table 1 *Overview of performance of different AGP variants.*

In figure 3, a comparison of dark current histograms with and without AGP for the 6x6 μm^2 pixel is given. Figure 4 shows the corresponding images in dark. The suppression of dark current by creating the hole layer at the interface equals a factor 80 at 60 ºC. In figure 5, the dark current as a function of the temperature is plotted. The temperature dependence is different for the different AGP pixels. More investigation is ongoing to explain this spread in temperature dependence. In figure 6, an Arrhenius plot of the pixel dark current for 1.0-1.0 implant configuration is depicted. This curve shows two different temperature regions. For temperatures above 300 K the thermal generation model with an activation energy of 0.72 eV describes the dark current. For temperatures below 273 K the dark current stabilizes at 0.06 pA/cm^2. For temperatures below 225 K no data is available. Electronic shuttering is functioning properly over the whole temperature region. More research is required to explain this stabilization at 0.06 pA/cm^2, but Takayanagi *et al.* [6] reported a similar behavior.

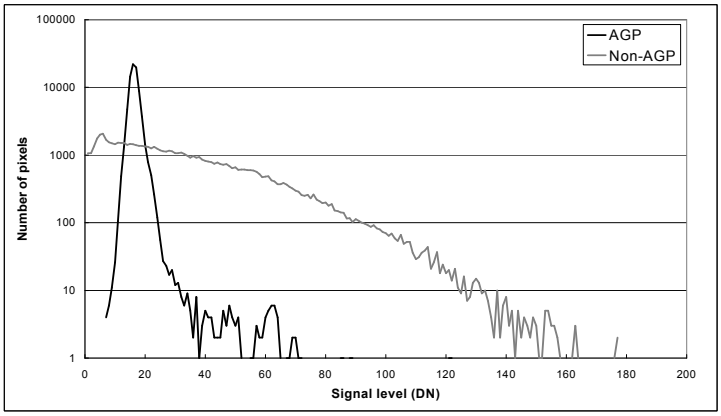

Figure 3 *Histogram of dark current at room temperature for 6x6 μm^2 pixel with and without AGP with an integration time of 6s.*

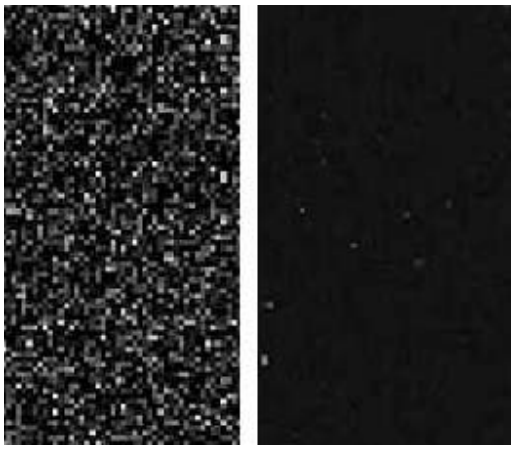

Figure 4. Dark images obtained under similar conditions without and with AGP (partial image only is shown)

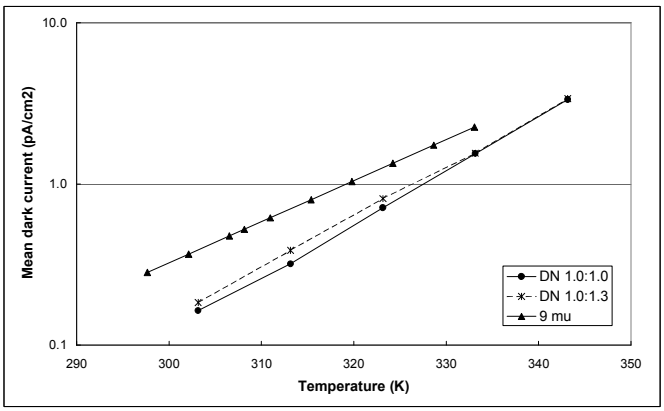

Figure 5 *Dark current of various AGP pixels versus temperature*

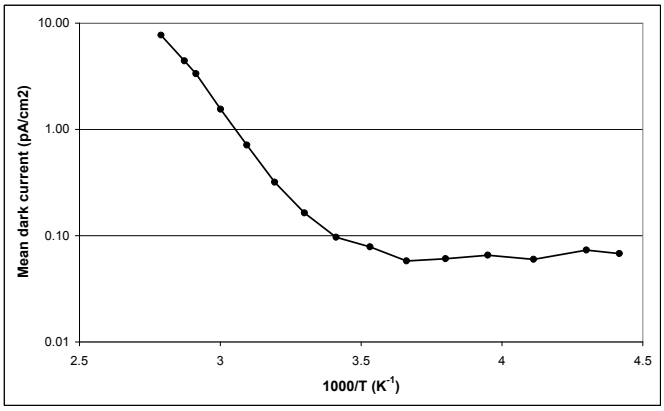

Figure 6 *Dark current of DN1-DN2=1.0-1.0 configuration versus reciprocal temperature*

Due to the very-low dark current levels, peaks of deep level traps are now clearly detectable as shown in figure 7. In figure 8, the Arrhenius plot of these 5 different peaks is shown and in table 2 the corresponding activation energies are given. An in-depth analysis of the origin of these deep level traps still needs to be performed.

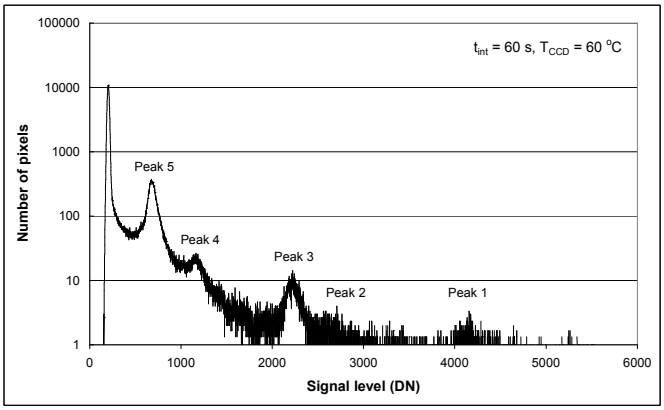

Figure 7 *Histogram of dark current of DN1-DN2=1.0-1.0 configuration at 60 ºC with 60 s integration time.*

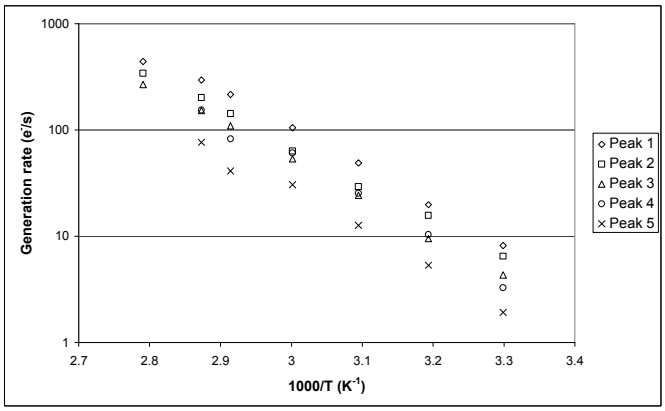

Figure 8 *Generation rate of deep level traps versus reciprocal temperature observed in dark current histograms*

Peak	Activation energy (eV)	Generation rate @ 60 ºC (e^-/s)
1	0.74	104.8
2	0.68	63.2
3	0.73	53.3
4	0.89	25.3
5	0.85	12.6

Table 2 *Properties of deep level traps observed in dark current histogram.*

Summary & Conclusions

We further improved the AGP concept for 6x6 μm^2 pixel resulting in, to the best of our knowledge, a new world-record dark current of 1.5 pA/cm^2 (3.4 e-/pixel/s) at 60 ºC. Other CCD parameters were not affected. This CCD AGP image sensor concept is well suited for applications requiring low noise levels without cooling, like professional digital photography, medical and scientific imaging.

Acknowledgements

The authors would like to thank their colleagues at DALSA Professional Imaging and DALSA Semiconductor for the support of this work.

References

1. J. Hynecek, "Virtual Phase Technology", *IEDM Technical Digest*, pp. 611-614, 1979
2. B.E. Burke and S.A. Gajar, "Dynamic Suppression of Interface-State Dark Current in Burried-Channel CCD's", *IEEE Trans. Electron Devices*, vol. 38, pp. 285-290, Feb. 1991
3. J. Bosiers, *et al.*, "A S-VHS compatible 1/3" 720(H) * 588(V) FT-CCD with low dark current by surface pinning", *Proc. IEDM'93* pp.97-100
4. I. Peters *et al*., "Dark current reduction in FF-CCDs", *2005 CCD & AIS Workshop*, Karuizawa, Japan
5. E.-J. Manoury *et al.,* "A 36×48mm^2 48M-pixel CCD imager for professional DSC applications, *Tech. Digest IEDM*, 2008.
6. Takayanagi *et al*., "Dark current reduction in stacked-type CMOS-APS for charged particle imaging", *IEEE Trans. Electron Devices*, vol. 50, pp. 70-76, 2003.