SDCRDAC24b

24-bit SD DAC

Features

- noise floor: -131 dBV (10 µHz – 1 Hz)
- noise floor: -128 dBV (1 Hz – 50 Hz)
- sample rate: 0-200 kS/s
- total out-of-band noise: < -60 dB
- quasi-differential output
- low latency: 4.25 µs
- radiation hardened
- total power consumption: 2.5 mW
- gain stability vs temperature: 1.5 ppm/K
- technology: UMC 0.18 µm CMOS
- silicon-verified
- design is scalable with regard to area and performance

Applications

- high-precision control systems
- automatic test equipment
- gain and offset adjustment/calibration
- programmable voltage and current sources
- process and servo control
- space applications
- high-quality audio (with minor scaling and other modifications to DAC)

General description

The SDCRDAC24b is a 24-bit sigma-delta charge-redistribution digital-to-analog converter (DAC). It is designed to have high absolute accuracy, low flicker noise and low power consumption, and it is robust against temperature variations and radiation. This makes the DAC ideally suited for demanding control applications in a wide variety of environments.

This product is silicon-verified.

Block diagram

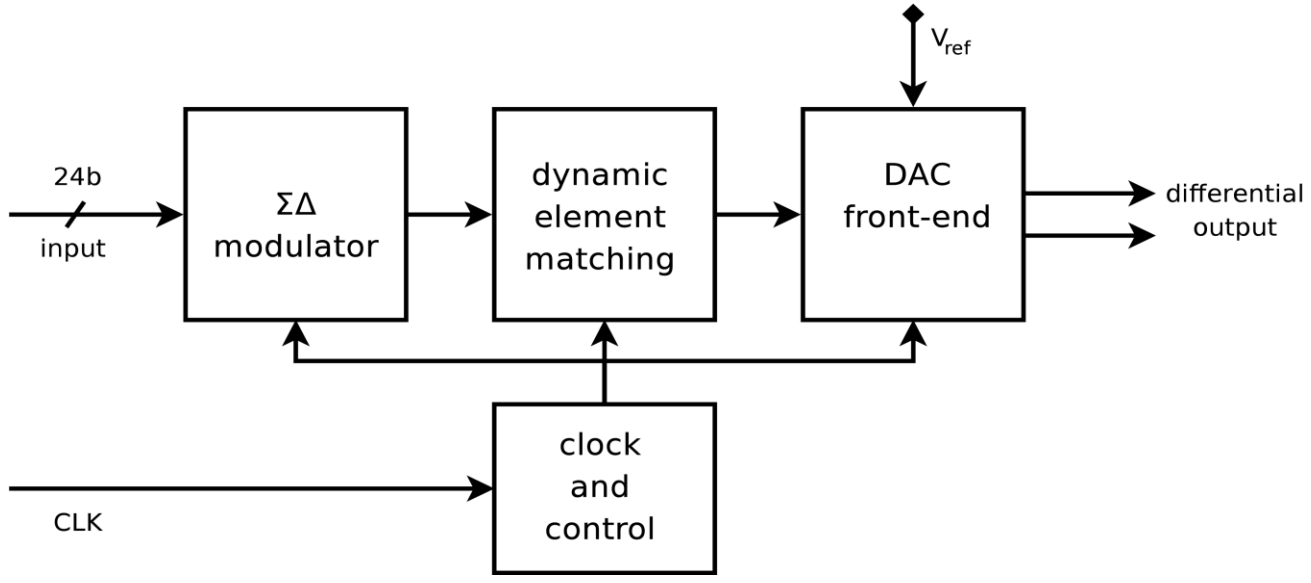

Figure 1: Block diagram

Specifications

V dig = 1.8V, V ref = 1.8V, fclk = 4MHz, unless noted otherwise

parameter	description	min	typ	max	units
Interfacing					
f_{CLK}	clock frequency	0	4		MHz
V_{dig}	digital supply voltage	1.6	1.8	2	V
V_{ref}	reference voltage	1	1.8	2	V
n	input data width		24		bits
$f_{s,in}$	update rate input data	0	100	f_{CLK}/20	S/s
$V_{out,max}$	output amplitude (differential)		2.14		V_{pp}
$V_{out,cm}$	DC output voltage (common-mode)		0.9		V
I_{ref}	current drawn from reference supply (1.8V)		400*		µA
I_{dig}	current drawn from digital supply (1.8 V)			970**	µA
Performance					
N_{LF}	noise floor (10 µHz – 1 Hz)		-131		dBV
N	noise floor (1 Hz – 50 Hz)		-128		dBV
OOBN	out-of-band noise: with load 1 MΩ // 1 nF unloaded or virtual-ground load unloaded or virtual-ground load, no dithering		 <-60 -65 -71		 dB dB dB
THD	total harmonic distortion with load 1 MΩ // 1 nF		 -83		 dBc
	gain stability vs. temperature with load 1 MΩ // 1 nF any load >1 MΩ		 -1.5	 7	 ppm/K ppm/K
V_0	offset voltage		135	150	µV
TID	total ionizing dose without effects on DAC output signal			>133	krad
SEE	single events without effects on DAC output signal (expected, not yet verified)			50	MeV·cm²/mg
Implementation					
N_{gates}	number of gates, including flipflops		5663		
Nflipfops	Number of flipflops		334		
Aanalog	die area of DAC front-end		1.18*		mm2
Atotal	Total die area, including digital, in UMC 0.18 µm CMOS		2.22*		mm2

* Both the current drawn from the digital supply I_{dig} and the area of the digital section will be lower when radiation resistance is not required and a standard digital library is chosen instead of a radiationhardened one. The area A_{analog} and the current I_{ref} drawn from the reference supply can be scaled down when higher noise levels are acceptable. See section 'Detailed description' for details.
** The current drawn from the digital supply I_{dig} includes the current for clock division and interface circuitry. Without this, I_{dig} is ~250 µA.

Detailed description

The SDCRDAC24b contains a second-order sigma-delta modulator which runs at $f_{CLK}/20$ or $f_{CLK}/80$. The design is measured using an OSR of 500 ($f_{s,in}$=100 S/s) but other input data rates are also possible. At low frequencies, 1/f noise is the dominant noise source, as visible in figure 3. At higher frequencies, noise performance is limited by thermal noise (designed to be 9 nV/√Hz), so the SNR scales with 3 dB/octave of signal bandwidth. Dithering is added to prevent tonal limit cycles. A dynamic element matching unit shapes the noise due to front-end element mismatch to out-of-band frequencies. The DAC is well suited to be included inside control loops, because the sigma-delta modulator has unity gain and no phase shift, and the latency is only 17 clock cycles (4.25 µs at f_{CLK}=4 MHz).

Upon request, scaled versions of the DAC are also available. The area of the analog section A_{analog} can be scaled in steps of a factor four. Roughly, a reduction of a factor of four results in 6 dB higher in-band noise, and 9 dB higher out-of-band noise.

As in any DAC, the output SNR is limited by the SNR of the reference voltage (since V_{out} = code·V_{ref}). In this DAC, the reference is not buffered internally, so the external reference needs to have a sufficiently high SNR. The reference is loaded by a switched capacitor (200 pF is fully charged, once every four clock cycles). Care has been taken to prevent code-dependent kick-back noise to the reference supply.

The switched-capacitor output of this DAC is not buffered internally, to enable a wide variety of applications and to minimize 1/f noise. The output is switched at a frequency of $f_{CLK}/4$, typically 1 MHz.

Typical applications

The SDCRDAC24b has been designed to directly deliver a voltage output to a buffer capacitor without requiring additional active filtering. This application is shown in figure 2. A load with an R_LC_L time constant of 1 ms (e.g. 1 MΩ // 1 nF) results in an out-of-band noise of lower than -60 dBc. The two 10 pF single-ended capacitors filter common-mode noise. With this voltage-mode output, the THD is ultimately limited by the linearity of the DAC capacitors. An alternative application is to inject the charge into the virtual ground input of a subsequent opamp stage, which will eliminate the dependence on capacitor linearity and therefore will improve linearity of the DAC.

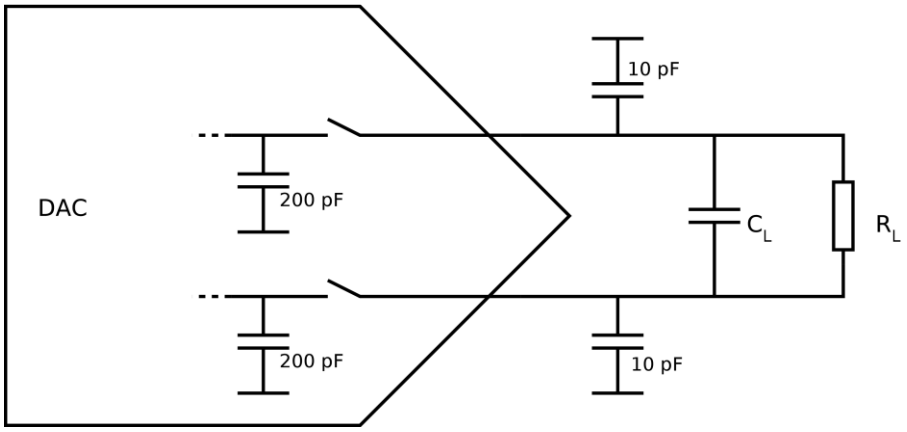

Figure 2: application with voltage-mode output

Typical performance characteristics

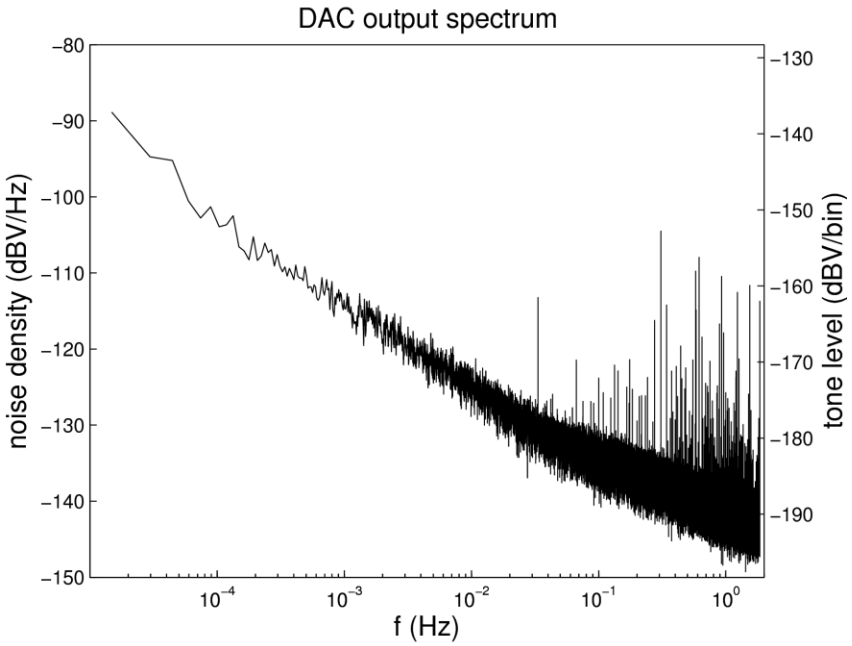

Figure 3: measured output spectrum

The measured output spectrum shown in figure 3 contains some spurious signals above 10mHz that are due to the measurement setup. Due to the long integration time these spurious tones appear much stronger than the noise, but their levels are actually lower than -153 dBV, far smaller than 1 LSB.

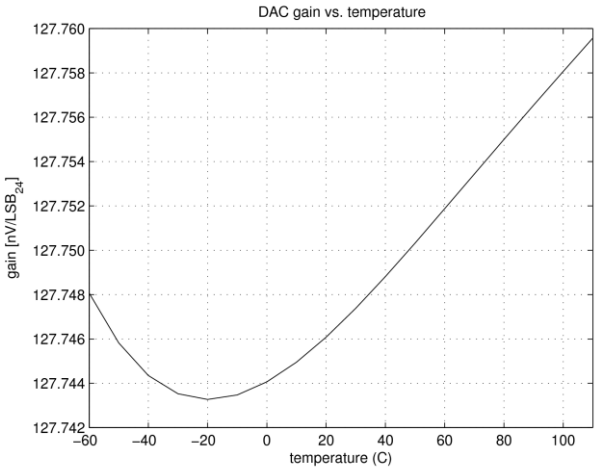

Figure 4: Typical DAC gain vs. temperature (load 1MΩ // 1nF)

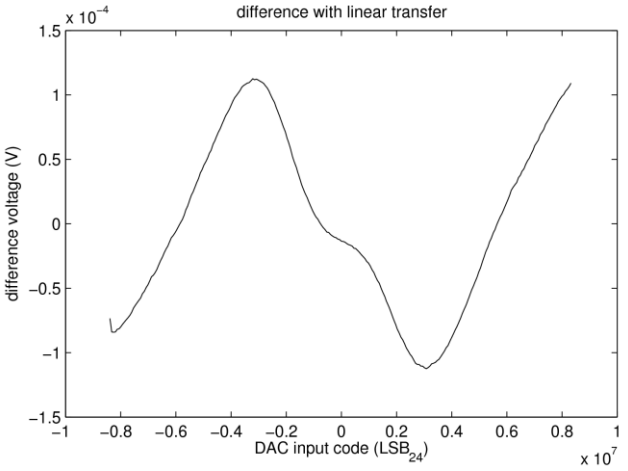

Figure 5: difference between measured DAC output and ideal linear transfer load (load 1MΩ // 1nF)

Port list

port name	width	description
data	24	Input data in 24-bits PCM format
clk	1	clock input
clk_LF	1	Modulator clock output; data sampled on rising edge
reset_n	1	Reset input, active low
pwrDwn	1	Power down input, active high
clkRatio	1	Selects oversampling ratio of modulator, active high
ditherEn	1	Enables dither generation in modulator, active high
Out_p	1	Analog output (positive)
Out_n	1	Analog output (negative)
VDDD	1	Supply for digital section (1.8 V)
GNDD	1	Digital ground
VDDA	1	Supply for analog section (1.8V)
GNDA	1	Analog ground
Vref	1	Reference voltage (1.8V)
GNDREF	1	Reference ground

Table 2: port function description

Note that these are only the external port names. When integrating the GDSII layout database for the analog front-end and the RTL code for the digital blocks of the DAC, some internal ports are used as well. These are described in detail in the documentation delivered with the IP.

Deliverables

In its current form, the IP block will be delivered as a combination of RTL code for the digital part and a layout database for the analog part. The total package contains:

- RTL code in VHDL for the digital part
- GDSII layout database of the DAC front-end
- abstract LEF file of the DAC front-end
- netlist of the DAC front-end, for behavioral modeling and layout verification
- documentation, including assembly guidelines
- test benches: RTL test bench for the digital part and a Verilog-A block that reads the digital output file into the analog simulation environment

Alternatively, Axiom IC can take care of the synthesis and place&route of the digital part, and deliver the complete IP block as a single GDSII layout database. Axiom IC engineers can also integrate the product as part of a SoC engagement in cooperation with the customer.

As mentioned under 'detailed description', other versions of this DAC, with scaled area and performance, can also be delivered. Upon request, the design can also be ported to other processes, as the circuit behavior is largely independent of technology. Please contact Axiom IC for more information.

Revision history

The following table lists the revision history, only major revisions are shown.

Revision	Date	Reason for revision
F2	2017-07-18	Template update
F1	2009-05-05	Initial version

Table 3: Document revision history

For more information about Teledyne DALSA visit our Web Site at

http://www.teledynedalsa.com/semi/mixed-signal/

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