Xcelera-CL+ PX8 Full

PCI Express x8 Frame Grabber

Key Features

- Half-length PCI Express x8 Board
- Acquires images from one Base, Medium or Full Camera Link® camera
- Rapid image acquisition and transfer rates beyond 1GB/s
- Supports Camera Link operations up to 85MHz
- Extended feature set supports advanced Camera Link pixel/tap configurations
- Windows® XP and Windows 7 (32/64-bit) compatible
- ROHS compliant
- On-board FPGA based real-time Bayer decoding and shading correction
- Power Over Camera Link (PoCL) Compliant
- Teledyne DALSA Platform Development Advantage – Free Run-time Licensing[1]

TRIGGER-TO-IMAGE RELIABILITY

Advanced PCIe x8 image acquisition

Building on the field proven technology and performance of Teledyne DALSA's X64 frame grabbers the new X64 Xcelera Series leverages the PCI Express (PCIe) platform to bring traditional image acquisition and processing technology to new levels of performance and flexibility.

The PCIe host interface is a point-to-point host interface allowing simultaneous image acquisition and transfer without loading the system bus and involving little intervention from the host CPU. Designed with the requirements of the machine vision OEMs in mind, the Xcelera Series will range from entry level frame grabbers, to high-performance image acquisition boards, to embedded vision processors.

Addressing the emerging needs of bandwidth-hungry machine vision applications, Teledyne DALSA's Xcelera Series is defining next generation frame grabber capabilities with the ability to deliver bandwidth beyond 1GByte/s over multiple-lane PCI Express implementations with room to grow.

The X64 Xcelera-CL+ PX8 Full is a Camera Link frame grabber that is based on the PCI Express x8 interface. Compatible with a Base, Medium or Full Camera Link® camera, the X64 Xcelera-CL+ PX8 Full supports a wide variety of multi-tap area and line scan colour and monochrome cameras. The X64 Xcelera-CL+ PX8 Full board can interface with advanced Camera Link camera output formats including 10-taps of 8-bit/pixel or 8-taps of 10-bit/pixel at 85MHz pixel clock rates.

The X64 Xcelera-CL+ PX8 Full has been built within Teledyne DALSA's Trigger-to-Image Reliability technology framework. Trigger-to-Image Reliability leverages Teledyne DALSA's hardware and software innovations to control, monitor and correct the image acquisition process from the time that an external trigger event occurs to the moment the data is sent to the host, providing traceability when errors do occur and permitting recovery from those errors.

Software Support

All of the frame grabbers in the Xcelera series are supported by Teledyne DALSA's Sapera Vision Software packages:

Sapera Essential, the core development platform, includes over 400 image processing primitive and industrial strength image analysis tools such as pattern finding, 1D and 2D barcode and OCR tools for part identification and detection, color processing tool, separation and measurement applications, blob analysis tool and inspection metrology tool for real-world dimensional measurements.

Teledyne DALSA Platform Development Advantage - Free Run-Time Licensing

The Sapera Essential standard processing tool run-time license is offered at no additional charge when combined with the Teledyne DALSA frame grabbers. This software run-time license[1] includes access to image processing functions, area-based (normalized correlation based) template matching tool, blob analysis and lens correction tool.

Sapera Nitrous accelerates Sapera Essential applications by providing a seamless support for graphical processing units (GPU) and multi-core CPUs optimization (MCO).

Sapera Architect Plus gives system integrators and industrial vision automation specialists a user-friendly, non-programming graphical environment to quickly prototype and test drive application specific imaging tools within Sapera Essential and Sapera Nitrous.

[1] Some conditions and limitations apply, contact Teledyne DALSA sales for details.

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X64 Xcelera-CL+ PX8 Full

PCI Express x8 Frame Grabber

Function	Description
Board	Camera Link Specifications Rev 1.2 compatible Half length PCI Express 1.1 x8 compliant ROHS Compliant
Acquisition	Supports one Base, Medium or Full Camera Link area and line scan camera Acquisition pixel clock rates from 20MHz to 85MHz
Resolution	Horizontal Size (min/max): 16 byte/256K bytes Vertical Size (min/max): 1 line/infinite lines for line-scan cameras 1 line/16million lines/frame for area-scan cameras Variable length frame size from 1 to 16 million lines for area-scan cameras 256MB onboard frame buffer memory Integrated advanced tap reversal engine allows independent tap formatting
Pixel Format and Tap configuration	Supports Camera Link tap configurations for 8, 10, 12, 14 and 16-bit mono or 8, 10 or 12-bit RGB For Base cameras in any of the following combinations: 3x8-bit/tap, 2x10-bits/tap, 2x12-bit/tap, 1x14-bit/tap, 1x16-bits/tap, & 1x24-bit/RGB For Medium camera - 4x8-bit/tap, 4x10-bits/tap, 4x12-bit/tap, 1x30-bit/RGB, & 1x36-bits/tap For Full—8x 8-bit/tap Camera Link; 10-tap/8-bit and 8-tap/10-bit configurations
Transfers	Real-time transfers to system memory Intelligent Data-Transfer-Engine automatically loads scatter-gather and tap description tables from the host memory without CPU intervention
On-board Processing	
Bayer Mosaic Filter	Hardware Bayer Engine supports one Camera Link Base 8, 10 or 12-bit Bayer Bayer output format supports 8, 10 or 12-bit RGB/pixel Zero host CPU utilization for Bayer conversion
Shading Correction	On the fly Flat-line and Flat-field correction with dead-pixel replacement Supports Camera Link Base, Medium or Full cameras User programmable calibration gain/offset maps
Output Lookup Tables	
Monochrome	Each input port has one 256x8-bit, 1024x10-bit, 4096x12-bit OLUTs
Colour	Each input port has one 8-bit in/out, 10-bit in 8 or 10-bit out, 12-bit in 12-bit/out Lookup table

Function	Description
Controls	Comprehensive event notification includes start/end of frame/transfer events Camera control signals for external event synchronization Optically isolated trigger inputs programmable as active high or low (edge or level trigger) TTL Strobes outputs PC independent serial communications ports provide support 9600 to 11500K baud Appear as system serial ports enabling seamless interface to host applications
Encoder Inputs	Web synchronization using TTL/RS422 compatible quadrature (AB) encoder Optically isolated input up to 200KHz RS422 input up to 5MHz
On-board GPI/Os[2]	4-optically isolated general purpose inputs tolerate 5 and 24VDC signals 4 general purpose outputs
Power Output	PoCL Compliant (4W max) Power-on-reset fused +12V output @ 1.5A +5V DC output at 1.5A
Software	Device driver supports: Micrsoft Windows XP and Windows 7 (32/64-bit) compatible Full support of Teledyne DALSA DIGITAL IMAGING's Sapera Essential, Sapera LT and Sapera Processing software libraries Application development using C++ and .Net languages(C++, C# or Visual Basic)
System Requirements	PCI Express Rev 1.1 compliant with one x8 slot system with 1024MB or higher system memory
Dimensions	6.375" (16.1cm) Length X 4.20" (10.7 cm) Height
Temperature	10°C (50° F) to 50° C (122° F) Relative Humidity: up to 90% (non-condensing)
Markings	FCC Class B—Approved CE—Approved

[2] Requires a separate slot for the bracket assembly

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