Features

- noise floor: < -139 dBV (10 µHz – 1 Hz)
- noise floor: -138 dBV (1 Hz – 50 Hz)
- noise floor: -113 dBV (20 Hz – 20 kHz)
- noise floor: -83 dBV (20 Hz – 1 MHz)
- input sample rate: 0-6 MS/s
- total out-of-band noise: < -64 dB without filtering
- low latency (down to 9 clock cycles): Ideal for closed loop applications
- wide common mode range
- quasi-differential outputs
- Outputs suitable for both current-mode and voltage-mode operation
- total power consumption: 1.5 mW (f_{CLK} = 6 MHz; P scales linearly with f_{CLK})
- gain stability vs temperature: < 2ppm/K
- low offset: < 3 µV
- offset stability vs temperature: < 30nV/K
- No code dependent loading of V_{ref}
- technology: UMC 0.18 µm CMOS
- silicon-verified
- design is scalable with regard to area and performance

General description

The SDCRDAC24bHBW is a 24-bit sigma-delta charge-redistribution digital-to-analog converter (DAC). It is designed to have high absolute accuracy, low noise and low power consumption, and it is robust against temperature variations. This makes the DAC ideally suited for high-performance audio as well as for demanding control applications in a wide variety of environments.

The product is based on the SDCRDAC24b, but this version is not radiation hardened. Instead, the SDCRDAC24bHBW has increased bandwidth, increased temperature stability and lower power consumption.

This product is silicon-verified.

Applications

- high-precision control systems
- automatic test equipment
- gain and offset adjustment/calibration
- programmable voltage and current sources
- process and servo control
- high-quality audio
- Active noise reduction systems

Block diagram

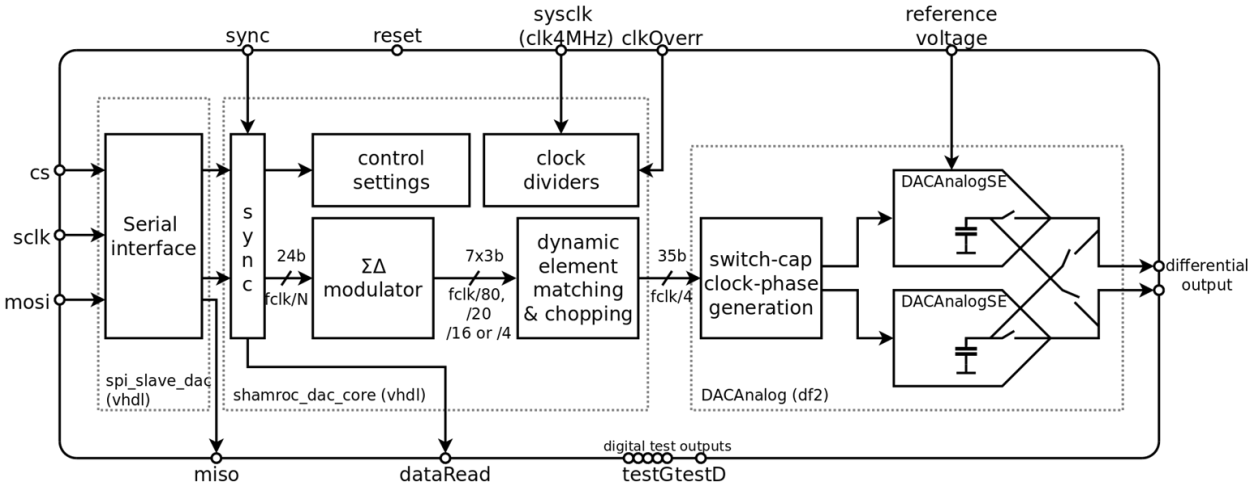

Figure 1: Block diagram

Ports list (of core IP block)

port name	width	description
Digital control signals		
clk	1	clock input
sync	1	input to synchronize internal counters, active high
reset	1	Reset input, active low
clkOverr	1	Clock-divider ratio override, active high
newData	1	Request input to read new input data, active high
dataRead	1	Acknowledge output, active low
Registered digital inputs		
data	24	Input data in 24-bits PCM format (two's complement)
pwrDwn	1	Power down input, active high
clkRatio	1	Selects clock-divider ratio for modulator
clkMult	1	Selects clock-divider ratio for modulator
choppingEn	1	Enables chopping of output, active low
ditherEn	1	Enables dither generation in modulator, active low
Analog outputs		
Out_p	1	Analog output (positive)
Out_n	1	Analog output (negative)
Power, ground and reference ports		
VDDD	1	Supply for digital section (1.8 V)
GNDD	1	Digital ground
VDDA	1	Supply for analog section (1.8 V)
GNDA	1	Analog ground
Vref	1	Reference voltage (1.8 V)
GNDREF	1	Reference ground

Table 1: Port function descriptions

Note that these are only the external port names. When integrating the GDSII layout database for the analog front-end and the RTL code for the digital blocks of the DAC, some internal ports are used as well. These are described in detail in the documentation delivered with the IP.

Pins (on the demonstrator IC)

On the demonstrator IC, a serial interface is present with which the registered digital input can be programmed. For this interface, the newData input takes the function of 'chip select' and is renamed accordingly. Following normal serial interface protocols such as SPI, the chip select is usually de-asserted (made high) after the completion of a transmission. This in effect signals to the DAC that new data has arrived. The interface is made such that it is also possible to be connected to serial digital audio interfaces, with very simple glue logic in between.

For more information on the interface or demonstrator IC, please contact TeledyneDALSA.

Specifications

Default Test Conditions

Digital supply voltage (V_{ddd})	1.8 V
Analog supply voltage (V_{dda})	1.8 V
IO voltage (V_{ddio} & data pins) [1)]	3.3 V
Reference voltage (V_{ref})	1.8 V
Input clock frequency	6 MHz
Load impedance	200 kΩ // 470 pF
Input sample rate (f_s)	48 kHz
Common mode output voltage (V_{cm})	0.9 V
Temperature (T)	25 ºC

Specifications

Parameter	Description	min	typ	max	units
f_{CLK}	clock frequency	0	6	>24	MHz
V_{ref}	reference voltage		1.8	1.98	V
V_{ddd}	digital supply voltage	1.62	1.8	1.98	V
V_{dda}	analog supply voltage	1.62	1.8	1.98	V
n	input data width		24		bits
$f_{s,in}$	update rate input data	0		f_{CLK}/4	S/s
T	operating temperature range	-55	25	110	ºC
DC characteristics					
$V_{out,max}$	Output voltage (differential), unloaded (V_{ref} = 1.8V)		2.25		V_{pp}
R_{out}	Low frequency output impedance (differential) [4)]		6.1		kΩ
G	Gain (V_{out}/LSB at V_{ref} = 1.8 V) unloaded loaded with 200 kΩ // 470 pF, f_{sig}=1 kHz		 134.4 127.9		 nV/LSB nV/LSB
INL	Integral non-linearity voltage mode		 20	 25	 µV
$V_{out,cm}$	DC output voltage (common-mode) voltage mode current mode acceptable range (THD deterioration < 2dB @ -10 dBFS; see Figure 13)	 -0.1	 0.9	 1.9	 V
I_{ref}	Current drawn from reference supply (1.8 V) [3)] [4)]		615		µA
I_{ddd}	Current drawn from digital supply (1.8 V) [4)]		200		µA
I_{dda}	Current drawn from analog supply (1.8 V) 4)		15		µA

Specifications (continued)

Parameter	Description	min	typ	max	units
AC performance					
N_{LF}	Noise floor 10 µHz – 1 Hz [2)] 1 Hz – 50 Hz 20 Hz – 20 kHz(A_{in}=-60dBFS un-wtd 200kΩ // 470pF) 20 Hz – 20 kHz(A_{in}=-60dBFS A-wtd 200kΩ // 470pF) 20 Hz – 200 kHz (200 kΩ // 470 pF) 20 Hz – 1 MHz (200 kΩ // 470 pF) 20 kHz – 1 MHz without filter (600 Ω // 280 pF)		 <-139 -138 -113 -116 -85 -83 -64		 dBV dBFS
THD	Total harmonic distortion (f_{in} = 1 kHz, 0 dBFS) high-ohmic load (200 kΩ // 470 pF) f_{CLK} = 3 MHz f_{CLK} = 6 MHz f_{CLK} = 12 MHz low-ohmic load (virtual ground [5)]) f_{CLK} = 3 MHz f_{CLK} = 6 MHz f_{CLK} = 12 MHz		 -92 -87 -74 -98 -114 -73		 dBc
THD+N	Total harmonic distortion + noise (f_{in}= 1kHz, 0dBFS) high-ohmic load (200 kΩ // 470 pF) f_{CLK} = 3 MHz f_{CLK} = 6 MHz f_{CLK} = 12 MHz low-ohmic load (virtual ground [5)]) f_{CLK} = 3 MHz f_{CLK} = 6 MHz f_{CLK} = 12 MHz		 -92 -87 -74 -95 -106 -73		 dBc
PSR	Power supply rejection 217 Hz square wave 200 mV_{pp} at V_{dda} 217 Hz (V_{in} = 0) 1 kHz +/- 217 Hz (f_{in} = 1 kHz, 0 dBFS) 217 Hz square wave 200 mV_{pp} at V_{ddd} 217 Hz (V_{in} = 0) 1 kHz +/- 217 Hz (f_{in} = 1 kHz, 0 dBFS)		 -108 -85 -117 -105		 dBV
ΔG/ΔT	Gain stability vs. temperature any load >1 MΩ			 ±2	 ppm/K
V_0	Offset voltage with chopping enabled without chopping		 0 ±3	 ±2 ±15	 µV
$\Delta V_0/\Delta T$	Offset drift over temperature with chopping enabled without chopping		 0	 -0.2	 µV/K

Specifications (continued)

Parameter	Description	min	typ	max	units
Implementation					
N_{gates}	number of gates, including flipflops		2742		
$N_{flipfops}$	Number of flipflops		492		
A_{analog}	die area of analog DAC front-end		1.18 3)		mm^2
A_{total}	Total die area, including decap and digital, in UMC 0.18 µm CMOS		1.72 3)		mm^2

Table 2: Specifications of SDCRDAC24bHBW

Notes:

1) The test chip uses 3.3V digital I/O signals, therefore an additional supply, V_{ddio} (3.3V), is implemented on the test chip.
2) f_{CLK} 4MHz; Z_{load} 1MΩ // 1nF (differential)
3) The area A_{analog} and the current I_{ref} drawn from the reference supply can be scaled down when higher noise levels are acceptable. See section 'Detailed description' for details.
4) I_{ref}, I_{dda} and I_{ddd} are proportional to f_{clk} ; R_{out} is inversely proportional to f_{clk}.
5) See Figure 17 for measurement setup; V_{cm}=0.2 V.

Typical Performance Characteristics

Low-frequency measurements

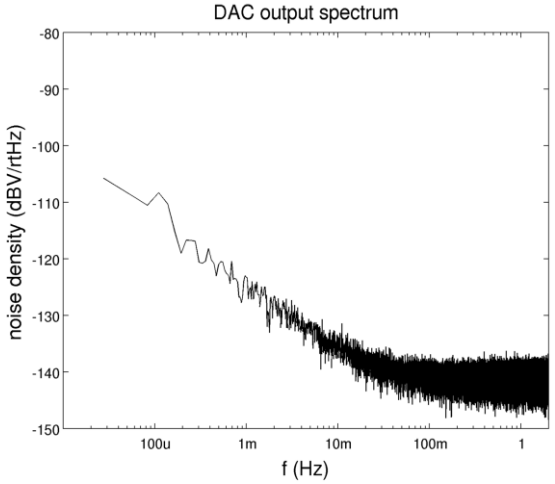

Figure 2: measured output spectrum
(f_{CLK} 4 MHz; note that the noise floor is limited by the measurement equipment, at least for the white part)

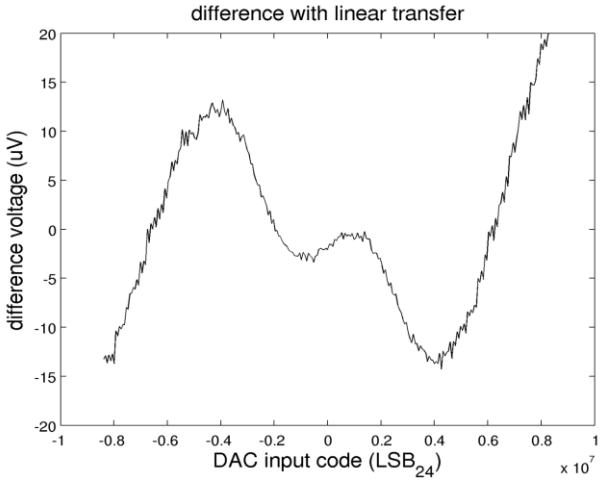

Figure 3: difference between measured DAC output and ideal linear transfer
(f_{CLK} 4 MHz; load 1 MΩ // 1 nF)

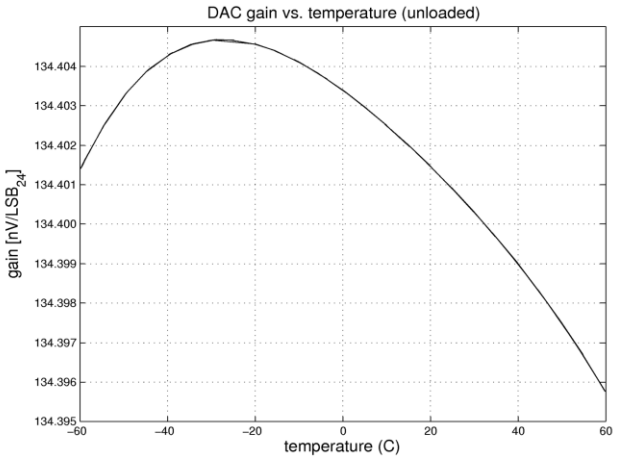

Figure 4: typical DAC gain vs. temperature
(f_{CLK} 4 MHz; unloaded)

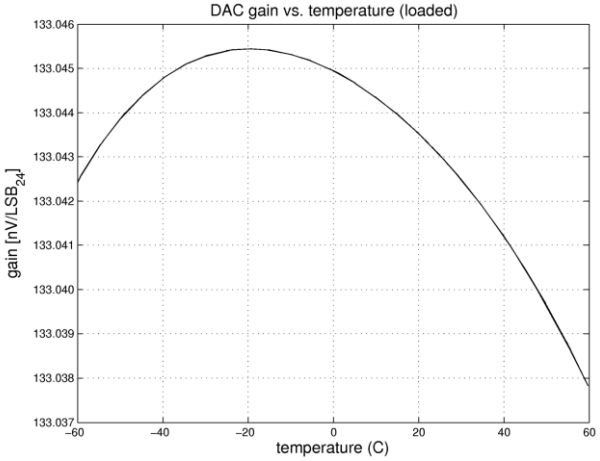

Figure 5: typical DAC gain vs. temperature
(f_{CLK} 4 MHz; loaded with 1MΩ // 1nF)

Audio-frequency measurements

The graphs below show measurement results.

Noise / output spectrum

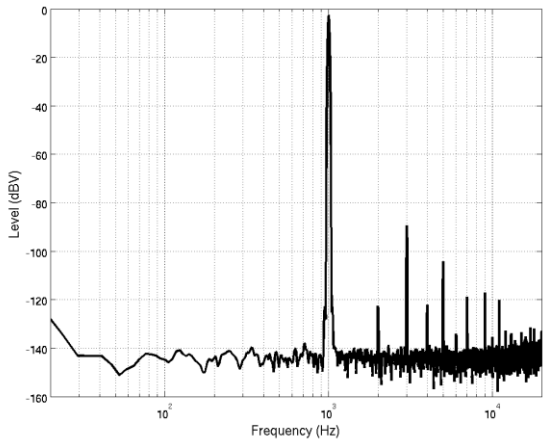

Figure 6 : Output spectrum in voltage mode
@ 0 dBFS input signal

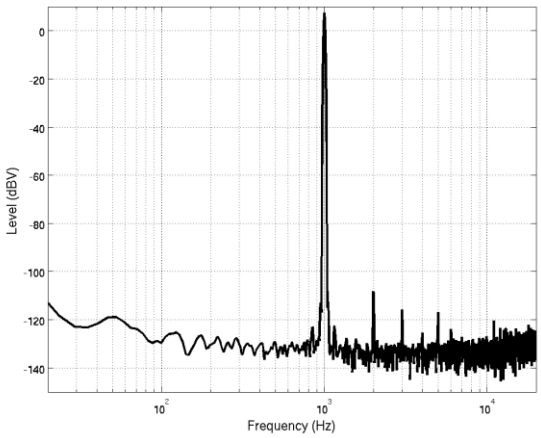

Figure 7 : Output spectrum in current mode
@ 0 dBFS input signal

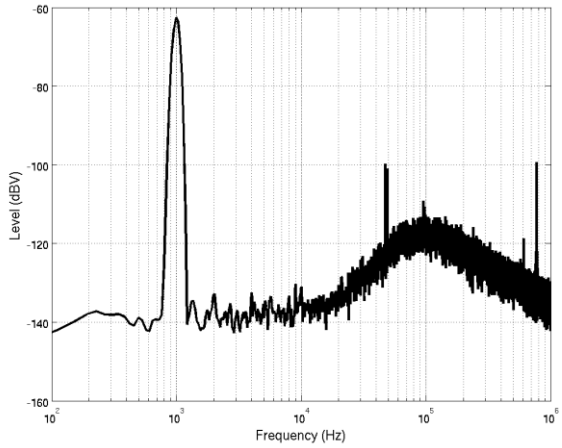

Figure 8 : Wideband output spectrum in voltage mode
@ -60 dBFS input signal

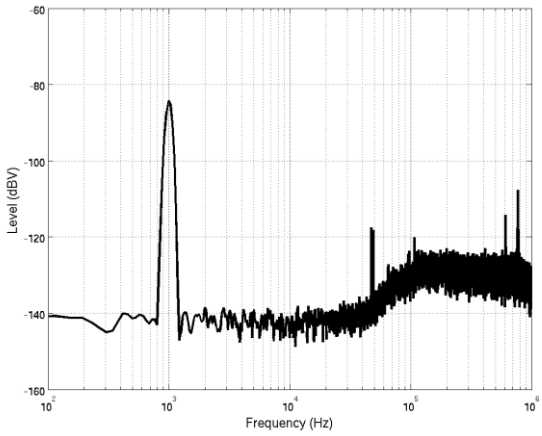

Figure 9 : Wideband output spectrum in voltage mode
without filter (600 Ω // 280pF) @ -60 dBFS input signal

THD+N

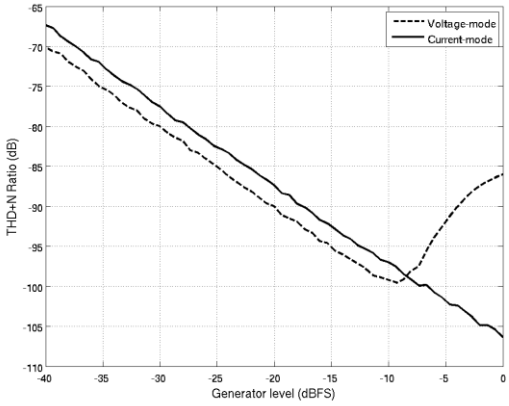

Figure 10 : THD+N @ 1kHz in both voltage mode and current mode as function of input level

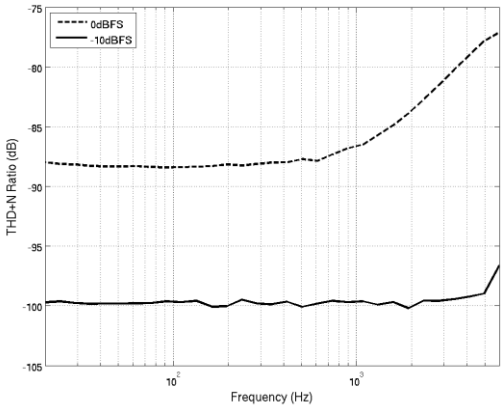

Figure 11 : THD+N Ratio in voltage mode as function of frequency

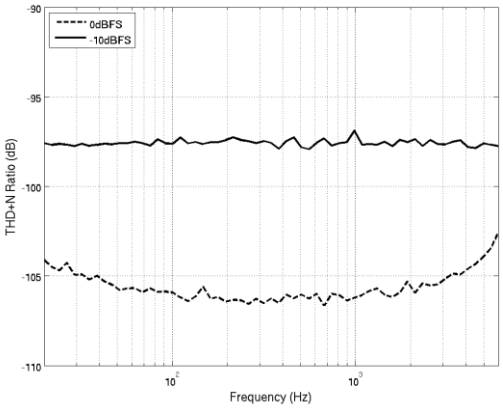

Figure 12 : THD+N Ratio in current mode as function of frequency

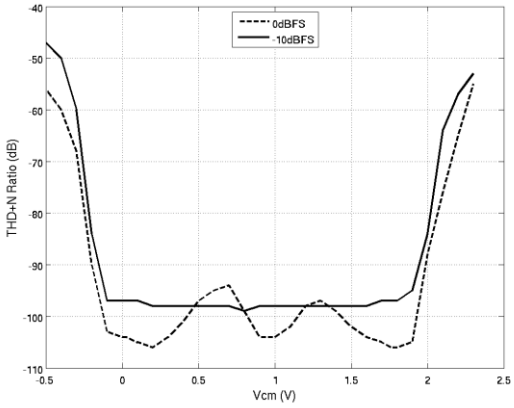

Figure 13 : THD+N Ratio in current mode as function of Vcm

Detailed description

The SDCRDAC24bHBW contains a second-order recursive sigma-delta modulator. Compared to a normal sigma-delta modulator, it has the advantage that the overall quantization noise is very low, both inside as well as outside the signal band. At very low frequencies, 1/f noise is the dominant noise source, as visible in figure 2. At higher frequencies, noise performance is limited by thermal noise (designed to be 10.5 nV/√Hz differential[1], at f_{CLK}=6 MHz), so the SNR scales with 3 dB/octave of signal bandwidth. Only above 20 kHz does the quantization noise becomes the dominant noise source, with a total energy that is below -64 dBFS (unloaded, without filtering). Dithering is added to prevent tonal limit cycles. A dynamic element matching unit shapes the noise due to front-end element mismatch to out-of-band frequencies. The DAC is well suited to be included inside control loops, because the sigma-delta modulator has a flat gain, no phase shift, and the latency is only 9 clock cycles (or 17 clock cycles when clock division ratio is set to 20 or 80).

As in any DAC, the output SNR is limited by the SNR of the reference voltage (since V_{out} = code·V_{ref}). In this DAC, the reference is not buffered internally, so the external reference needs to have a sufficiently high SNR. The reference is loaded by a switched capacitor (200 pF is fully charged, once every four clock cycles). Care has been taken to prevent code-dependent kick-back noise to the reference supply.

The switched-capacitor output of this DAC is not buffered internally, to enable a wide variety of applications and to minimize 1/f noise. The switched capacitor output can either directly be used as voltage output (see Figure 16), or can be fed into the virtual ground of an external Op-Amp (see Figure 17). In the former case, the offset and 1/f noise of the system is very low, but the linearity is limited by the non-linear voltage dependence of the on-chip DAC capacitors (as visible in Figure 3). With an Op-Amp, the linearity can be improve by feeding the DAC output current into a virtual ground node. Note that the DAC has a wide range of tolerable voltage potential for this virtual ground node. See the 'typical application' section for more details.

Scalability

Upon request, scaled versions of the DAC are also available. The area of the analog section A_{analog} can be scaled in steps of a factor four. Roughly, a reduction of a factor of four results in 6 dB higher in-band noise, and 9 dB higher out-of-band noise.

Timing behavior

The DAC internally generates a number of clock signals that are a ratio of the externally supplied system clock. The backend of the data-path, being the dynamic element matching and the DAC itself, has a fixed ratio of 4. The four clock cycles are used to complete one cycle of the switched capacitor DAC, as it uses a special multiple phase clocking scheme to get constant reference current consumption.

The front-end of the datapath, with the sigma-delta modulator and the dither generation, have a programmable period of N cycles, depending on the control settings as shown in Table 3. The lower frequency modes (N = 20 or 80) are useful for low-speed applications; these modes lower the digital power consumption and improve the resilience towards mismatch (as the dynamic element matching algorithm always runs at the highest speed, and thus oversamples the sigma-delta modulator output when N > 4).

The high frequency modes (N = 4 and to a lesser extend also N = 16) are useful for applications where the signal bandwidth is higher (compared to the clock-frequency), such as audio applications.

[1] 2*kT/C/BW=2*kT/100pF/750kHz

clkOverr input	*clkMult control setting*	*clkRatio control setting*	**Clock ratio N**
0	0	0	80
0	0	1	20
0	1	0	16
0	1	1	4
1	x	x	4

Table 3: Control bits that determine the clock ratio of the sigma-delta modulator

To maximize the flexibility with all these clock-ratios, the DAC can operate in two modes, which are discussed below.

DAC as timing master

In the first mode of operation, the DAC is the timing master and dictates when the data in the input register is actually read (sampled). In this mode, the transfer of data follows a typical asynchronous protocol where the chip-select input functions as a request and the 'dataRead' output functions as an acknowledge. The timing of the signals in this mode is shown in Figure 14.

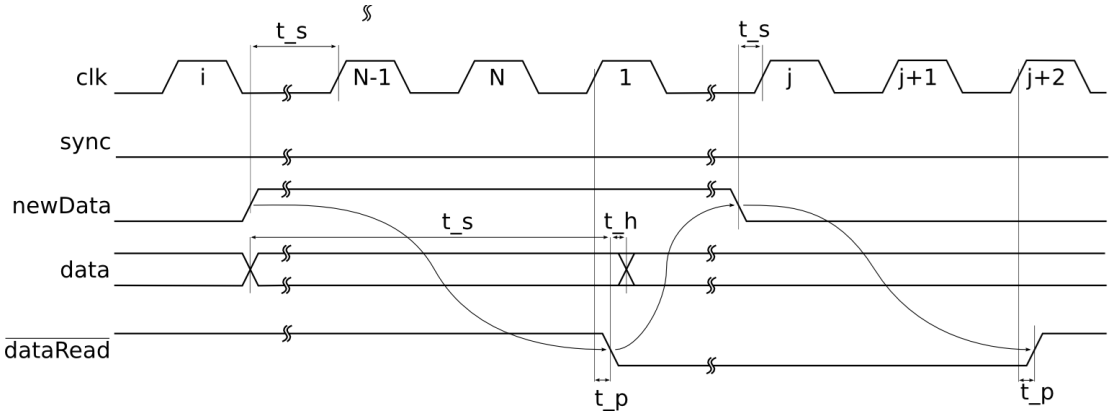

Figure 14: Timing behavior in asynchronous master timing mode

When 'newdata' is made high (meaning that the transfer of a new word to the DAC has been completed), then the DAC waits until its internal counters trigger a new sample moment at which the data in its input register is read into the sigma-delta modulator. This data-read is acknowledged by making the 'dataRead' low. After the dataRead goes low. The dataRead remains low until a few clock cycles after the chip-select is made low again for a new cycle.

In this mode, data transfers can be completely asynchronous, as a synchronizing element is added between the clock domain of the serial interface and the clock domain of the system clock, to avoid chances on metastability. For this reason, there is a delay between a rising edge of chip-select and an acknowledge (it will take at least three rising edges of the system clock until the chip-select edge is acknowledged).

The user can choose whether it justs updates the DAC value when it seems fit (for 'static value' applications such as feed forward actuator control) or the user can send a new data word every *M*N* system clock cycles for equidistant sample intervals (for accurate reproduction of time-varying signals). For equidistant sampling, care has to be taken that *N* equals the programmed clock ratio, as tabulated in Table 3 above.

DAC as timing slave

The alternative mode of operation is that the DAC acts as a timing slave, to let the application dictate the timing phase of the samples. In this case, the user should assert the 'sync' input for one clock cycle every time a new sample is available. Such a synchronization pulse resets the internal counters and leads to an immediate acknowledge by dataRead. The timing of the signals is shown in figure 15.
In this timing mode, it is even more important that the sync pulses only occur at N*M intervals. Pulses at other intervals break the normal state cycle pattern for the DAC, which can lead to an undefined output sample (after which, the DAC returns to its normal behavior).

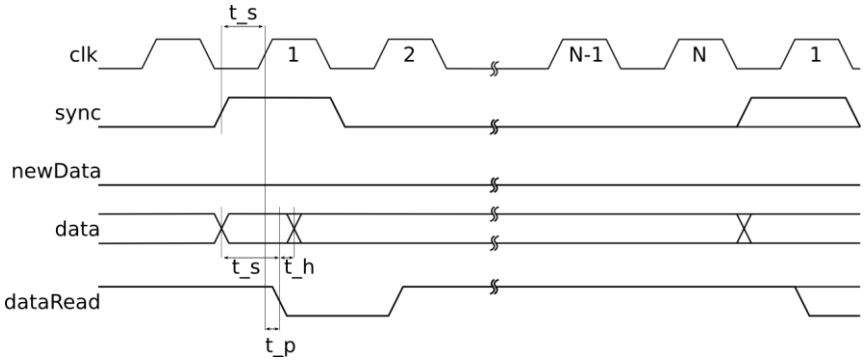

Figure 15: Timing behavior in (legacy) slave timing mode

The two modes can also be combined, with simultaneous activation of 'newData' and 'sync'. A scenario for such a situation to occur can for example be that the user asserts VDH_SSI_Sync only at the first sample after startup, to ensure a known delay between the arrival and capture of the input data. In this case the response from cycle 1 (the cycle where VDH_SSI_Sync is active) and onwards will be the same as in Figure 14.

Typical applications

The SDCRDAC24bHBW has been designed to directly deliver a voltage output to a buffer capacitor without requiring additional active filtering. This application is shown in Figure 16. Here, the output voltage is stored on a hold capacitor C_L in between refreshes from the switched capacitor DAC, which occur every 4 clock cycles. When the output is loaded by a resistive load, then one should take care that the ripple in leakage/charge cycle is kept low enough for the application. As an indication: with f_{CLK} = 4MHz, meaning a DAC refresh rate of 1 MHz, a load with an R_LC_L time constant of 1 ms (e.g. 1 MΩ // 1 nF) results in an out-of band ripple lower than -60 dBc. The two 10 pF single-ended capacitors filter common-mode noise. With this voltage-mode output, the THD is ultimately limited by the linearity of the DAC capacitors.

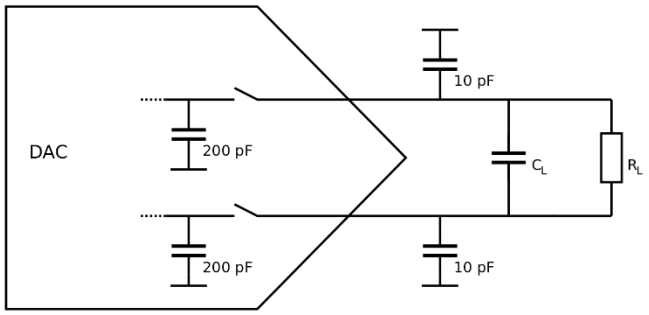

Figure 16 : Application with voltage mode output

An alternative application is to inject the charge into the virtual ground input of a subsequent opamp stage, which will eliminate the dependence on capacitor linearity and therefore will improve linearity of the DAC. See Figure 17.

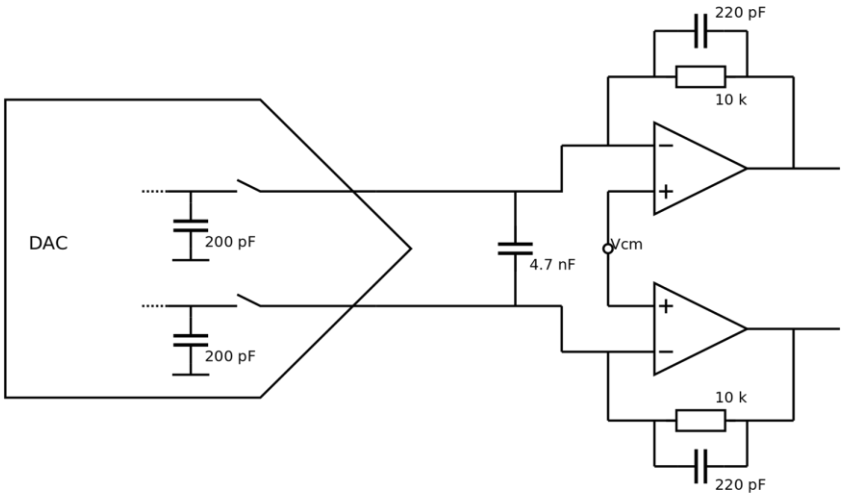

Figure 17 : Application with current mode output

Deliverables

In its current form, the IP block will be delivered as a combination of RTL code for the digital part and a layout database for the analog part. The total package contains:

- RTL code in VHDL for the digital part
- GDSII layout database of the DAC front-end
- abstract LEF file of the DAC front-end
- netlist of the DAC front-end, for behavioral modeling and layout verification
- documentation, including assembly guidelines
- test benches: RTL test bench for the digital part and a Verilog-A block that reads the digital output file into the analog simulation environment

Alternatively, Axiom IC can take care of the synthesis and place&route of the digital part, and deliver the complete IP block as a single GDSII layout database. Axiom IC engineers can also integrate the product as part of a SoC engagement in cooperation with the customer.

As mentioned under 'detailed description', other versions of this DAC, with scaled area and performance, can also be delivered. Upon request, the design can also be ported to other processes, as the circuit behavior is largely independent of technology. Please contact Axiom IC for more information.

Revision history

Revision	Date :	Reason for revision
F1	2010-05-20	Preliminary version
F2	2010-12-21	Updated with more measurment results
F3	2011-07-11	Minor updates
F4	1017-07-20	New template

For more information about Teledyne DALSA visit our Web Site at

http://www.teledynedalsa.com/semi/mixed-signal/

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