# Robust Design of a Dynamically Controlled Low-Power Level-up Shifter Operating up to 300V

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*Abstract*: **A new low-power level-up shifter circuit is presented. This circuit produces a digital output signal in the 0 – 300V range from a digital input signal in the 0 – 5V range. The proposed circuit reduces power through two key features: Dynamic charge control reduces the power dissipated in the level-up stage, and a "break before make" logic reduces the short-circuit power of the output stage. Detailed design methodology and optimized circuits for different voltage ranges are described in this paper. This circuit is designed under DALSA Semiconductor's 0.8µm 5V/HV CMOS/DMOS technology. Simulation results validate its operation and performance.**

## I. INTRODUCTION

In the last few years, high-voltage and "smart power" integrated circuits have attracted much interest. They target a growing market spurred by a wide range of applications, including display drivers, automotive electronics, small DC motor control, switching regulators and telecommunication circuits. Driven by the need to reduce the size of electronic boards and maintain high reliability, the operating supply voltage for high voltage applications are increasing steadily, ranging up to 300V. Level-up shifter circuits are widely used as output drivers for interfacing logic and functional devices or circuits, such as MEMS devices [1][2] and flat panel display (e.g. plasma display, electroluminescent display) [3][4]. Availability of low-power level-up shifter is important for portable equipments, especially for devices requiring high voltage level shifting.

Several silicon manufacturers offer high voltage processes that combine low-voltage (LV) standard CMOS logic with high-voltage (HV) output buffers on the same chip. In this paper, the proposed level-up shifter is designed in a 0.8µm 5V/HV CMOS/DMOS technology offered by DALSA Semiconductor. It is a modular smart power technology based on a 0.8µm standard CMOS process. This technology also provides high voltage DMOS transistors that can support up to 300V. It is a thin gate oxide technology, which limits the typical gate-source voltage to 5V. The circuit presented in this paper may contain 4 different types of MOS transistors, as shown in Fig. 1.

Device (a) is a high-voltage N channel DMOS, device (b) is a high-voltage P channel DMOS. Both devices (a) and (b) can withstand a high voltage of up to 300V between their source and drain electrodes. Devices (c) and (d) are standard low voltage NMOS and PMOS for normal 5V operation (used in CMOS control logic). Moreover, they can be floated up to 50V with respect to the substrate potential, which means they can serve as active loads in voltage mirrors when the high voltage power supply is lower than 50V. If the high voltage power supply is higher than 50V, we must use HV DMOS transistors.

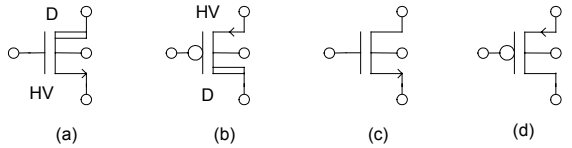


Fig. 1. Example of devices: (a) HV NDMOS (b) HV PDMOS (c) LV NMOS (d) LV PMOS

## II. OPERATION OF A LEVEL-UP SHIFTER

### *A. General Architecture of a Level-up Shifter*

The general architecture of a high-voltage level-up shifter is shown in Fig. 2. It is similar to a simple CMOS inverter, except for gate connection [5]. The gate of HV NDMOS $M_1$ can be readily controlled by the low-voltage levels 0 and $V_{dd}$, where $V_{dd}$ is the low-voltage power supply. The gate of the HV PDMOS $M_2$ needs a level shift to operate between $V_{pp}$ and $V_{pp}$-$V_{dd}$, where $V_{pp}$ is the high voltage power supply. The level-up shifter is composed of three parts: output stage ($M_1$ and $M_2$), level-up stage and control logic.

As far as power consumption of the level-up shifter is concerned, except the dynamic power charge/discharge to the load capacitance, the major contributions to power consumption are the power of the level-up stage and short-circuit power of the output stage. Various methods have been proposed to minimize the static current consumption of the level-up stage [1, 3, 4, 5]. With respect to the area of HV ICs, HV DMOS transistors tend to dominate the required area. Minimizing the number of HV DMOS transistors in the level-up shifter circuit is one of the most important aspects for reducing the required area.

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*B. Operation of the Proposed Circuit*

In this paper, we minimize the power dissipation of the level-up stage using the dynamic charge control concept, and

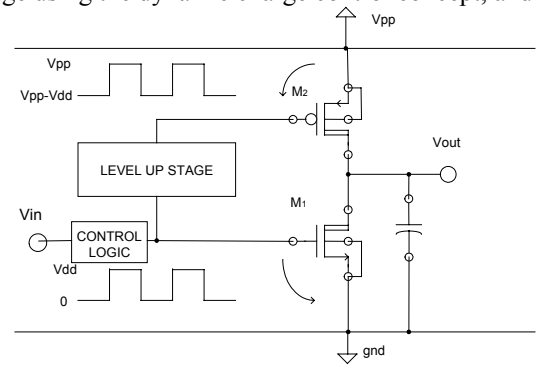


Fig. 2. General architecture of a HV level-up shifter

minimize the short-circuit current of the output stage using the so called "break before make" concept. In addition, we only use 4 HV DMOS transistors in the level-up stage, which is fewer than previous works [1, 3, 5]. On the other hand, the proposed circuit can work up to 300V by selecting the suitable type of HV DMOS transistors. The proposed circuit and the corresponding simulation results are shown in Fig. 3 and Fig. 4, respectively.

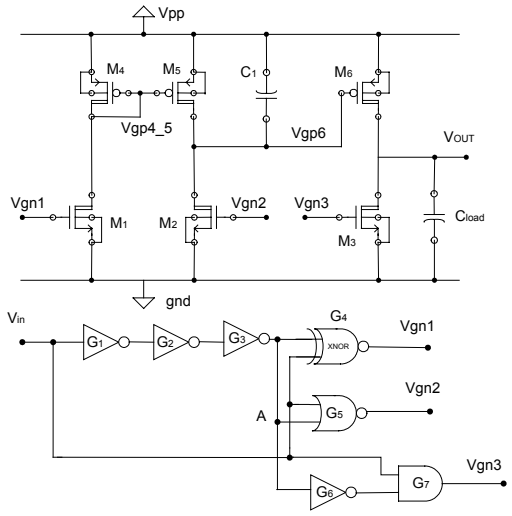


Fig. 3. Schematic of the proposed circuit

The proposed circuit is composed of an output stage ($M_3$ and $M_6$), a level-up stage ($M_1$, $M_2$, $M_4$, $M_5$ and $C_1$) and LV control logic ($G_1$ – $G_7$). The operation of the level-up shifter is controlled by $V_{gn1}$, $V_{gn2}$, and $V_{gn3}$, which are derived from the same input signal $V_{in}$.

When $V_{in}$ goes high, $V_{gn1}$ receives a pulse of short duration $\tau$ (delay of $G_1$ to $G_3$). It turns on transistor $M_1$, and causes a voltage drop of 5V across the load transistor $M_4$. The 5V drop across $M_4$ turns on $M_5$ and discharges the capacitor $C_1$, thus, bringing $V_{gp6}$ to $V_{pp}$, which then turns off the output transistor $M_6$. After $M_6$ is switched off, $V_{gn3}$ goes high, which turns on the output transistor $M_3$. When the $V_{gn1}$ pulse finishes, transistors $M_1$, $M_2$, $M_4$ and $M_5$ are all turned off. Node gp6 is isolated from the rest of the circuit (only

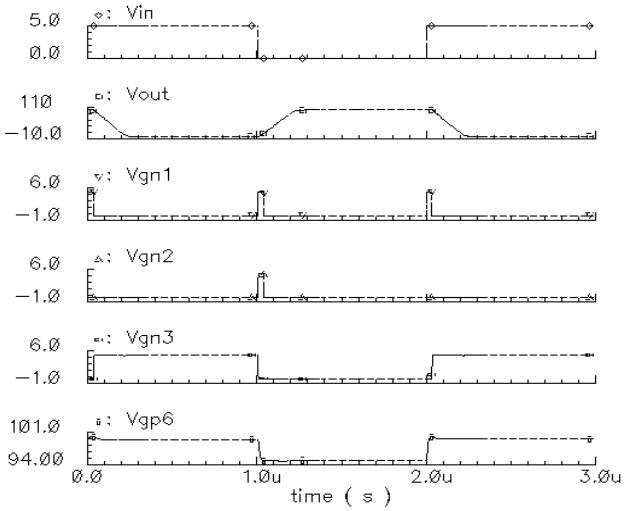


Fig. 4. Simulation results of the proposed circuit

high impedance connected to this node), and the charge stored in capacitor $C_1$ and the gate capacitor of $M_6$ will not change. When $V_{in}$ goes low, $V_{gn3}$ goes low immediately, which turns off output transistor $M_3$. Then, both $V_{gn1}$ and $V_{gn2}$ are pulsed for short duration $\tau$, which turns on transistors $M_1$ and $M_2$. Because $M_1$-$M_2$, $M_4$-$M_5$ are identical, there is a 5V drop across $M_4$ and $M_5$, which turns on the output transistor $M_6$. After a short duration $\tau$, both $V_{gn1}$ and $V_{gn2}$ go low almost at the same time (in fact, $V_{gn2}$ is slightly delayed) and transistors $M_1$, $M_2$, $M_4$ and $M_5$ are turned off. Node gp6 is also isolated from the rest of the circuit, and charge stored in node gp6 keeps $V_{gp6}$ at $V_{pp}$-5V, as needed for the level-up circuit to operate correctly.

From this discussion, the level-up stage only conducts for a short duration $\tau$ when input signal makes a transition, which significantly decreases the power dissipation of the level-up stage. On the other hand, the output transistors $M_3$ and $M_6$ are never turned on at the same time, which minimizes the short-circuit power of the output stage. Simulation results show that the power of the level-up stage and short-circuit power of the output stage can reduced to 5% of the total power consumption of the circuit (condition: $V_{pp}$=300V, $C_{load}$=32pF, which is the load of test probe).

## III. DESIGN METHODOLOGY

*A. Feedthrough From the Output Node*

From simulations, we find that the $V_{gp6}$ waveform has the following features: When $V_{gn1}$ goes high, $V_{gp6}$ is pulled up to $V_{pp}$ and $M_6$ is turned off, the output signal $V_{out}$ decreases from $V_{pp}$. When $V_{gn1}$ goes low, $V_{gp6}$ has a voltage drop $\Delta V$ from $V_{pp}$, and this voltage drop mainly occurs when output transistor $M_6$ is in the triode region (Fig. 5b). In addition, $\Delta V$ depends on the value of capacitor $C_1$: the smaller the capacitor $C_1$, the bigger the voltage drop $\Delta V$. If $\Delta V$ is too large, such as more than 0.8V (the threshold voltage of HV PDMOS), the

output transistor $M_6$ will be turned on, thus causing short circuit current in the output stage.

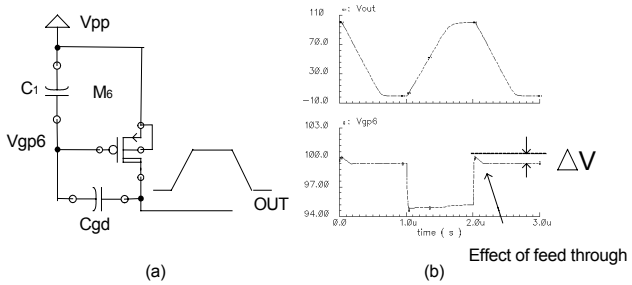


Fig. 5. Effects of feedthrough from the output node: (a)Principle (b) Waveform

This phenomenon is due to the feedthrough from the output node. $V_{gp6}$ is sensitive to the switching of the high voltage output node through the gate-drain Miller capacitance $C_{gd}$ of HV PDMOS transistor $M_6$ (Fig. 5a). If we ignore the parasitic capacitors in node gp6 because of their small values, the voltage drop is shown in (1).

$$\Delta V = \frac{C_{gd}}{C_1 + C_{gd}} \Delta V_{out} \tag{1}$$

$C_{gd}$ is mainly due to the oxide capacitance when $M_6$ is in the triode region. Indeed, $C_{gd}$ decreases significantly in the saturation region, because it is equal to a depletion capacitance in series with an oxide capacitance [6]. Therefore, $\Delta V$ mainly happens when $M_6$ is in the triode region. From the I-V curve of HV PDMOS, we learn that $V_{ds\text{-}sat}$ is 20 Volts. We can use the above formula to find the minimum capacitance $C_1$. For example, to have $\Delta V<0.6V$ (the threshold voltage of HV PDMOS is 0.8V), we need $C_1 > 32.3C_{gd}$ (capacitance in the triode region).

*B. The Timing of Control Signals*

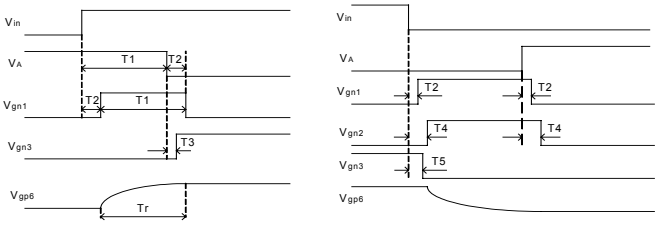


Fig. 6. Waveforms of the control signals: (a) Input rising edge (b) Input falling edge
$T_1$: delay of $G_1 - G_3$, $T_2$: delay of $G_4$, $T_3$: delay of $G_6$, $G_7$
$T_4$: delay of $G_5$, $T_5$: delay of $G_7$, Tr: rising time of $V_{gp6}$

Special attention was paid to determine the timing requirements:

*Case 1, Timing requirements to ensure the "break before make" operation*. For the input rising edges, the waveforms of control signals are shown in Fig. 6a. In order to avoid output transistors $M_3$ and $M_6$ turning on at the same time, we must respect the following relation:

$$T_r < T_1 - T_2 + T_3 \qquad \text{if } T_3 < T_2 \tag{2}$$

For the input falling edges, the waveforms of control signals are shown in Fig. 6b. For the same reasons, we have:

$$T_5 < T_4. \tag{3}$$

*Case 2, Timing requirements between $V_{gn1}$ and $V_{gn2}$.* From the operation of this circuit, we know that, ideally, $V_{gp6}$ is equal to $V_{pp} - 5V$ when the output transistor $M_6$ is turned on. In order to keep $V_{gp6}$ at that value, $M_5$ and $M_2$ should be turned off at the same time. Considering the delay between $V_{gn1}$ and $V_{gp4\_5}$, the timing requirements of $V_{gn1}$ and $V_{gn2}$ are shown in Fig. 7.

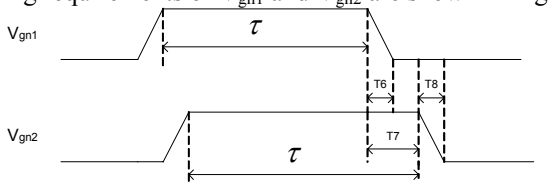


Fig. 7. Timing constraints between $V_{gn1}$ and $V_{gn2}$.

$T_6$: falling time of $V_{gn1}$, $T_7$: delay between $V_{gn2}$ and $V_{gn1}$, $T_8$: Falling time of $V_{gn2}$. $\tau$: high duration of $V_{gn1}$ and $V_{gn2}$.

Assume 10% variation on $V_{gp6}$ is acceptable, then we must have $V_{pp}$-5.5V<$V_{gp6}$<$V_{pp}$-4.5V. From simulations, the required timing parameters $T_6$, $T_7$ and $T_8$ are related as in the Fig. 8. ($C_1$=3p). The grey area defines a safe operating region. We can design the circuit such that timing parameters $T_6$, $T_7$ and $T_8$ are in the safe operating region. For example: 0.5ns<$T_6$<1.5ns, 1.2ns<$T_7$<2.25ns, 0.5ns<$T_8$<2.75ns. (shown in the arrow region of Fig. 8)

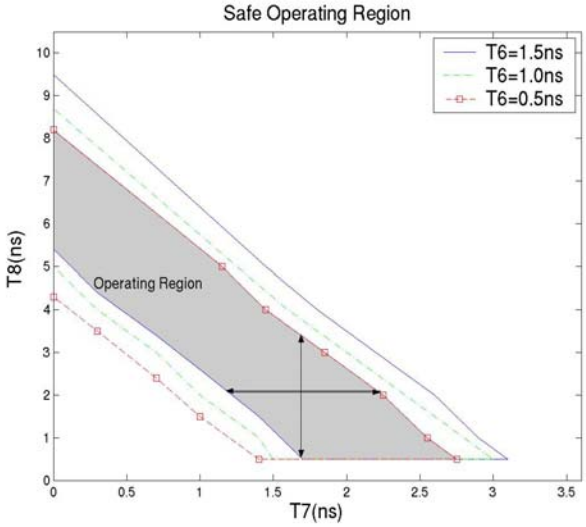


Fig. 8. Timing safe operating region

The safe timing operating region changes with capacitor $C_1$ (simulation results are shown in Fig. 9). The bigger the capacitance $C_1$ is, the wider the safe operating region becomes. It facilitates design and improves the circuit robustness. On the other hand, a bigger capacitance increases power consumption, and it requires more time to charge and discharge.

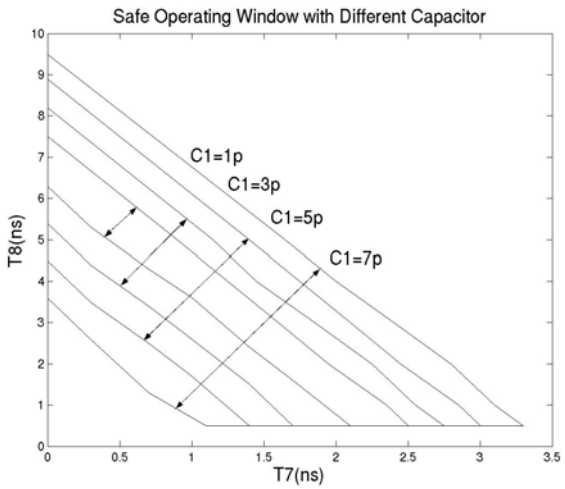


Fig. 9. Relation between Safe operating regions and $C_1$

*C. Design Validation*

The circuit could fail if the voltage drop of $M_5$ is large enough to exceed the gate-source breakdown voltage of $M_6$, or too small to turn on $M_6$. Undesired voltages on $V_{gp6}$ may be due to incorrect timing relation between $V_{gn1}$ and $V_{gn2}$. Consequently, we should carefully design the timing parameters $T_6$, $T_7$ and $T_8$ in the safe operating region, while considering the process variations. Unfortunately, there are only typical HV DMOS model in the library. We used an approximate method to verify the robustness against process variations of HV DMOS transistors. We assumed the transconductance mismatch between HV NDMOS and HV PDMOS is +/-10% and +/-2% between same type HV transistors. This mismatch can be simulated by applying different high-level voltage to $V_{gn1}$ and $V_{gn2}$. The following give some design corner examples. One is when the transconductance of $M_1$ and $M_2$ is 10% higher than typical values, the other is when transconductance of $M_1$ is 10% lower than typical values and transconductance of $M_2$ is 14% lower than typical values.

For the LV components, we should consider the following design corners: Low-voltage transistors corners (fast n – fast p, fast n – slow p, slow n – fast p, slow n – slow p), Capacitor $C_1$ corners (fast, slow). We can combine the above HV DMOS corners with the low voltage components corners and simulate them. A robust design should guarantee the circuit could work at all corners. The simulation results of all combined corners show the $V_{gp6}$ vary from $V_{pp}$-6V to $V_{pp}$-4.3V, and the circuit operates correctly.

Another consideration is the minimum operating frequency. Indeed, node of gp6 is a dynamic node. Thus, a small subthreshold/leakage current from $M_5$ ($V_{gs}$ of $M_5$ is about 0.5V-0.6V) and leakage current from $M_2$ will charge/discharge this dynamic node. This limits the minimum operating frequency of this level-up circuit.

*D. Design for Different Voltage Ranges*

Because LV transistors can be floated up to 50V and the breakdown voltages of different types of high-voltage transistors are different, there are some minor differences in the circuit when operating with different voltage range. First, for the high-voltage power supply range from 20V to 50V, we can replace the active load HV transistors $M_4$ and $M_5$ by LV transistors, which can save about 25% area. Second, for the power supply range from 50V to 100V, we can use any type of HV transistors in the output stage according to the circuit specification, and we should chose a suitable type of HV NDMOS/PDMOS transistor pair in the level-up stage, which have 5V drop in the active load. Third, for the HV voltage from 100V to 300V, there are only one HV NDMOS and one HV PDMOS that can support it. In order to have 5V drop in the active loads, each active load $M_4$ (or $M_5$) should be replaced by two HV PDMOS transistors in parallel.

## IV CONCLUSION

The high voltage level-up shifter presented in this paper reduces power through a dynamic charge control concept and a "break before make" concept. The design methodology followed in this work aims at implementing a robust design. This methodology includes timing design of control signals, approximate design corners validation, selecting capacitor $C_1$ by considering the feedthrough from the output node, determination of safe operating regions, and voltage range specific optimizations. The simulation results show that the dynamic power for charging/discharging the load capacitance can be up to 95% of total power consumption of the circuit ($V_{pp}$=300V, $C_{load}$=32pF). Moreover, this circuit only uses 6 HV transistors in a configuration that works up to 300V.

## ACKNOWLEDGMENTS

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