CRDAC 12b

12 bit charge-redistribution DAC

Features

- Fixed gain of +2 or -1
- Supply voltage 1.5 to 5V
- Load impedance □ 16Ω
- $SNR_{@5mW}$ 101dB
- $THD_{@5mW,1kHz}$ 0.03%
- 0.125mm² in 0.14µm CMOS

Applications

- Cellular Phones / Music Phones
- Smart Phones
- Portable Media / MP3 Players
- Portable CD / DVD Players

General description

This data sheet describes a general purpose headphone amplifier (HPA) in a 140nm CMOS process.

The amplifier can drive loads down to 16Ω and with a supply voltage ranging from 1.5 Volt to 5 Volt.

With the internal feedback resistors the gain of the amplifier is +2 or -1 depending on which input is used.

Block diagram

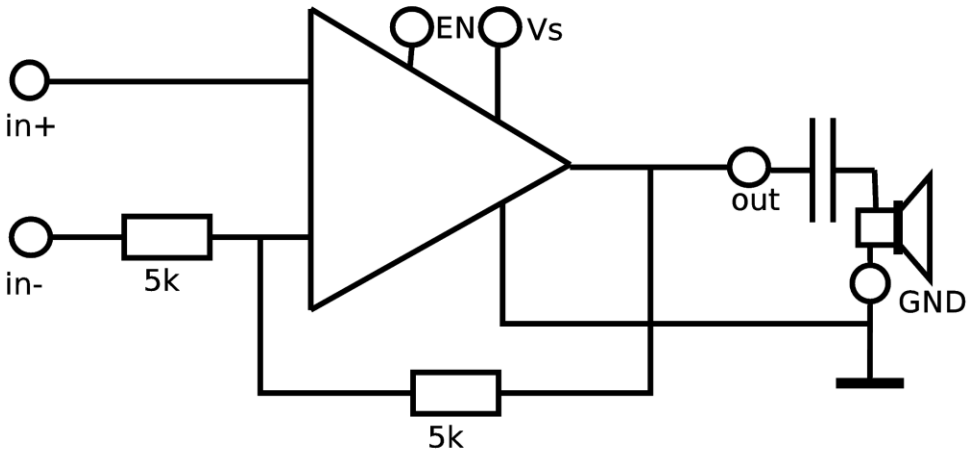


Figure 1: Block diagram headphone amplifier

Detailed description

The headphone amplifier (HPA) is a class AB amplifier in a standard 180nm CMOS process.
The input requires a DC bias network to set the output voltage at half the supply voltage Vs/2. This biasing network must be decoupled to ground for an optimal PSRR.

Applications with DC coupling ('true ground' application) are possible when a positive and a negative supply voltage are used (+/-0.75V to +/-2.5V). It must be noticed that the substrate of the chip is connected to the negative supply pin. Combining the HPA with other circuits that are designed for a single supply voltage on the same chip is not possible when those circuits make use of the same 'signal' ground. Such a combination is possible when a P-well is added for the NMOS transistors as a process option.

Specifications

V_{S+}=1.8V, R_{LOAD}=32Ω, $P_{OUT@1\%THD}$, T=25°C unless otherwise noted.

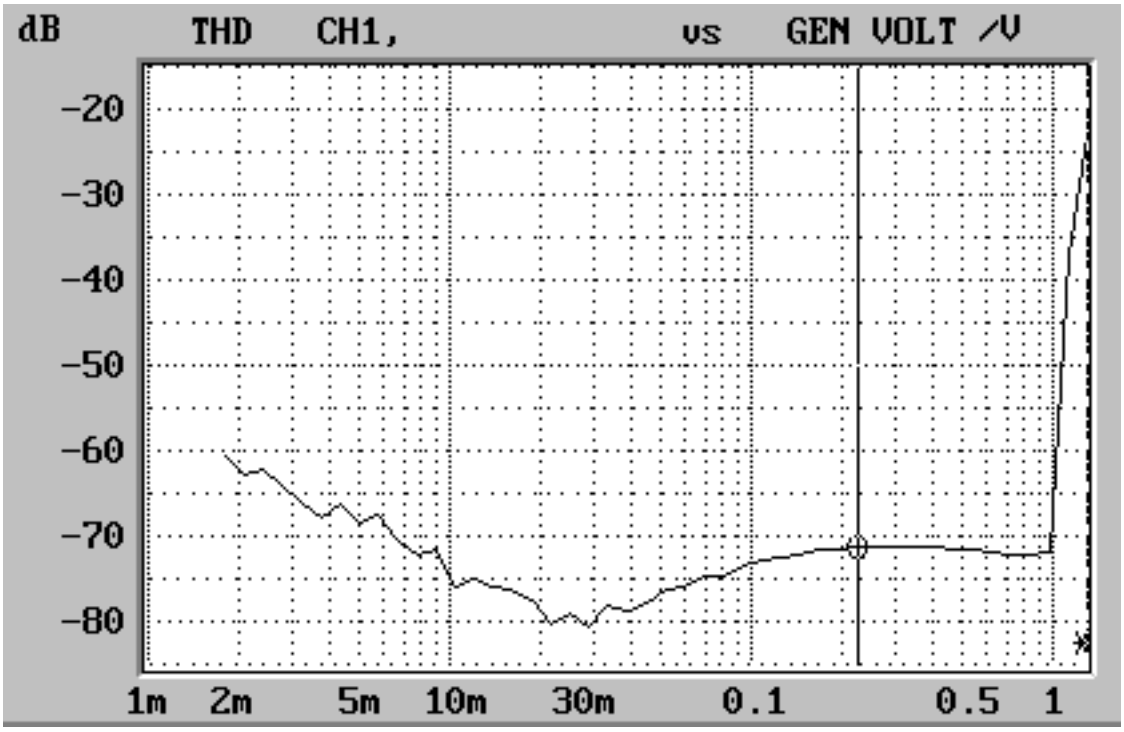
Parameter	Description	Min	Typ	Max	Units
Supply					
V_{S+}	Supply voltage	1.5	1.8	5	V
I_Q	Quiescent current		1		mA
Performance					
P_{OUT}	Output power		10		mW
$P_{OUT@16\Omega}$	Output power at 16Ω, V_{S+} =1.8V		19		mW
$P_{OUT@16\Omega,Vs=3.3V}$	Output power at 16Ω, V_{S+} = 3.3V		69		mW
THD	Distortion at P_{OUT} = 5 mW, 1 kHz		0.03		%
SNR_{MAX}	Signal to Noise Ratio at P_{OUT} = 5 mW, 1 kHz BW = 20kHz		101		dB
V_{NOISE}	Output noise, BW = 20kHz		2.5		µV
$PSRR_{@1kHz}$	Power Supply Rejection Ratio at 1kHz		51		dB
$PSRR_{@217Hz}$	Power Supply Rejection Ratio at 217Hz		51		dB
R_{LOAD}	Allowed load impedance	16			Ω
Implementation					
A_{C18}	Chip area in CMOS 140nm		0.125		mm^2

Table 1: Specifications

Typical Characterisics

Measured THD
inverting mode (gain=-1)

Supply = 3.3V, R_{LOAD} = 32Ω, input = 1kHz sine, T = 25°C



Port list

Port name	width	Description
in+	1	Non-inverting input
in-	1	Inverting input
out	1	Output
EN	1	Enable (active high)
Vs	1	Positive supply
GND	1	Ground

Table 2: Port function descriptions

Deliverables

The product can be delivered as a single IP component for customer integration or Axiom IC engineers can integrate the product as part of a SoC engagement. A GDSII layout (version F1) is available for these purposes.

Revision history

Revision	Date:	Reason for revision
F1	2010-04-27	Initial version
F2	2017-07-20	Template update

For more information about Teledyne DALSA visit our Web Site at

http://www.teledynedalsa.com/semi/mixed-signal/

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