A Dynamically Controlled and Refreshed Low-Power Level-up Shifter

Zhengrong Huang, Yvon Savaria, Mohamad Sawan
École Polytechnique de Montréal, Groupe de Recherche en Microélectronique
huang@grm.polymtl.ca, yvon.savaria@polymtl.ca, mohamad.sawan@polymtl.ca

Abstract: A low-power level-up shifter circuit is presented. This circuit produces a digital output signal in the 0 – 300V limits from a digital input signal in the 0 – 5V range. The proposed circuit reduces power consumption through two key features: Dynamic charge control decreases the power dissipated in the level-up stage, and a "break before make" logic reduces the short-circuit power of the output stage. An asynchronous control circuit is designed to refresh the dynamic node so that the proposed circuit can work at any low frequency. Detailed design methodologies are described in this paper. This circuit is designed and implemented under DALSA Semiconductor's 0.8μm 5V/HV CMOS/DMOS technology. Simulation results validate its operation and performance.

I. INTRODUCTION

In the last few years, high-voltage and "smart power" integrated circuits have attracted much interest. They target a growing market spurred by a wide range of applications, including display drivers, automotive electronics, small DC motor control, switching regulators and telecommunication circuits. Driven by the need to reduce the size of electronic boards and maintain high reliability, the operating supply voltage for high voltage applications are increasing steadily, ranging up to 300V. Level-up shifter circuits are widely used as output drivers for interfacing logic and functional devices or circuits, such as MEMS devices [1][2] and flat panel display (e.g. plasma display, electroluminescent display) [3][4]. Availability of low-power level-up shifter is important for portable equipments, especially for devices requiring high voltage level shifting.

Several silicon manufacturers offer high voltage processes that combine low-voltage (LV) standard CMOS logic with high-voltage (HV) output buffers on the same chip. In this paper, the proposed level-up shifter is designed in a 0.8μm 5V/HV CMOS/DMOS technology offered by DALSA Semiconductor. It is a modular smart power technology based on a standard CMOS process. It is a thin gate oxide technology, which limits the typical gate-source voltage to 5V. The circuit presented in this paper may contain 4 different types of MOS transistors, as shown in Fig. 1 Device (a) is an N channel HV DMOS, and device (b) is a P channel HV DMOS. Both devices (a) and (b) can withstand a high voltage of up to 300V between their source and drain electrodes. Devices (c) and (d) are standard low voltage NMOS and PMOS for normal 5V operation.

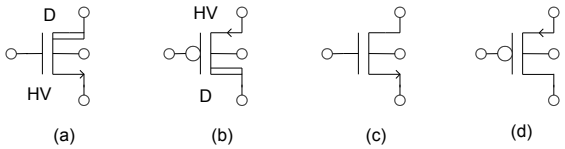


Fig. 1. Available devices: (a) HV NDMOS (b) HV PDMOS (c) LV NMOS (d) LV PMOS

II. OPERATION OF A LEVEL-UP SHIFTER

A. General Architecture of a Level-up Shifter

The general architecture of a high-voltage level-up shifter (LUS) is shown in Fig. 2. It is similar to a simple CMOS buffer, except for gate connection [5]. The gate of HV NDMOS M_1 can be readily controlled by the low-voltage levels 0 and V_{dd}, where V_{dd} is the low-voltage power supply. The gate of the HV PDMOS M_2 needs a level shift to operate between V_{pp} and V_{pp}-V_{dd}, where V_{pp} is the high voltage power supply. The LUS is composed of three parts: an output stage (M_1 and M_2), a level-up stage and control logic.

As far as power consumption of the LUS is concerned, except the dynamic power charge/discharge to the load capacitance, the major contributions to power consumption are the power of the level-up stage and short-circuit power of the output stage. Various methods have been proposed to minimize the static current consumption of the level-up stage [1, 2, 3, 4]. With respect to the area of HV ICs, HV DMOS transistors tend to dominate the required area. Minimizing the number of HV DMOS transistors in the LUS circuit is one of the most important aspects for reducing the required area, as DMOS transistors are much larger than minimum size LV transistors.

B. Operation of the Proposed Circuit

The power dissipation of the level-up stage is minimized using the dynamic charge control concept, and we minimize the short-circuit current of the output stage using the so called "break before make" concept [7]. An asynchronous control circuit is designed to refresh the dynamic node, enabling operation at very low frequency (down to DC). In addition, we only use 4 HV DMOS transistors in the level-up stage, which is less than in previous works [1, 3, 5]. The proposed circuit and the corresponding simulation results are shown in Fig. 3 and Fig. 4, respectively.

The proposed circuit comprises an output stage (M_3 and M_6), a level-up stage (M_1, M_2, M_4, M_5 and C_1) and the required LV control logic ($I_1 – I_{21}$). The operation of the

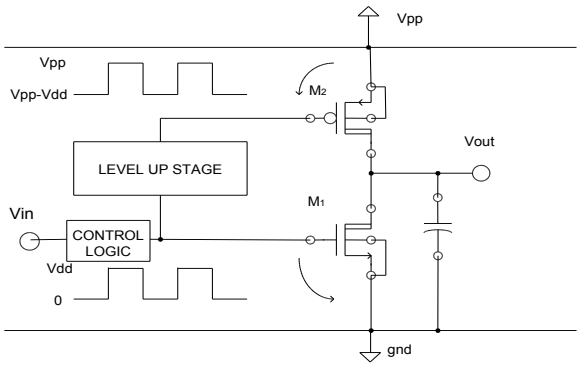


Fig. 2. General architecture of a HV level-up shifter

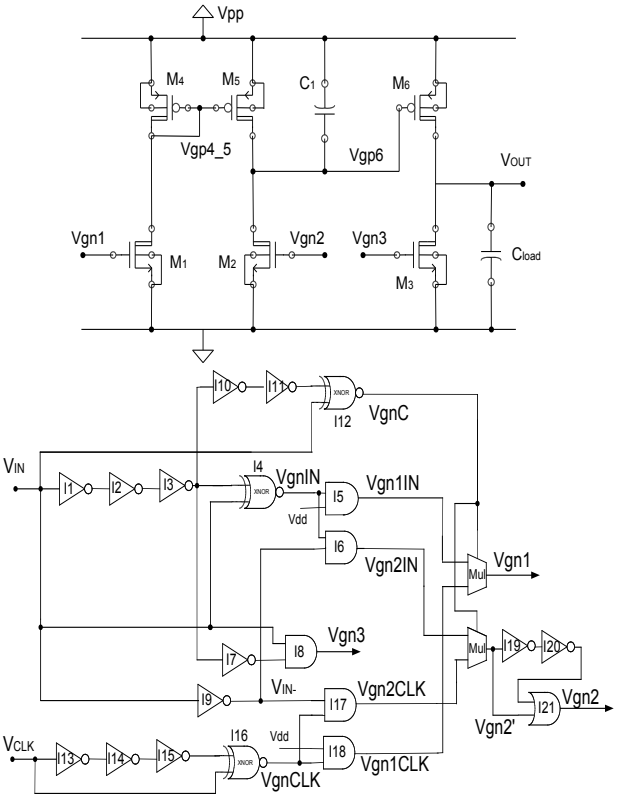


Fig. 3. Schematic of the proposed circuit

level-up shifter is controlled by V_{gn1}, V_{gn2}, and V_{gn3}, derived from input signal V_{IN} and refresh clock signal V_{CLK}.

When V_{IN} goes low, V_{gn3} goes low after the delay of I_8, which turns off output transistor M_3. V_{gn1IN} and V_{gn2IN} receive a pulse of short duration τ_1 (delay of I_1 to I_3) and V_{gnC} receives a pulse of short duration τ_2 (delay of I_1 to I_3 and I_{10}, I_{11}). V_{gnC} controls two multiplexers such that V_{gn1IN} and V_{gn2IN} are selected to V_{gn1} and V_{gn2}, respectively. Then, V_{gn1} and V_{gn2} turn on transistors M_1 and M_2. Because M_1-M_2, and M_4-M_5 are matched, the induced 5V drop across M_4 and M_5 is used to turn on the output transistor M_6. After a short duration τ_1, both V_{gn1} and V_{gn2} go low almost at the same time (in fact, V_{gn2} is slightly delayed) and transistors M_1, M_2, M_4 and M_5 are turned off. The node gp6 is isolated from the rest of circuit (only high impedance connected to this node), and charge stored in node gp6 keeps V_{gp6} at V_{pp}-5V. After a short duration τ_2, V_{gnC} goes low, and V_{gn1CLK} and V_{gn2CLK} are selected to V_{gn1} and V_{gn2} for refresh operation. When V_{IN} goes high, V_{gn1IN} receives a pulse of short duration τ_1, V_{gn2IN} is disabled by V_{IN-} and V_{gnC} receives a pulse of short duration τ_2. Then, V_{gn1IN} is passed to V_{gn1}, which turns on transistor M_1, and causes a voltage drop of 5V across the load transistor M_4. The 5V drop across M_4 turns on M_5 and discharges capacitor C_1, which brings V_{gp6} to V_{pp}, and consequently turns off output transistor M_6. After M_6 is switched off, V_{gn3} goes high, which turns on the output transistor M_3. When the V_{gn1} pulse finishes, transistors M_1, M_2, M_4 and M_5 are all turned off. Node gp6 is isolated from the rest of the circuit, and the charge stored in capacitor C_1 and the gate capacitance of M_6 will not change. After a short duration τ_2, V_{gnC} goes low, and V_{gn1CLK} is selected to V_{gn1} for refresh operation.

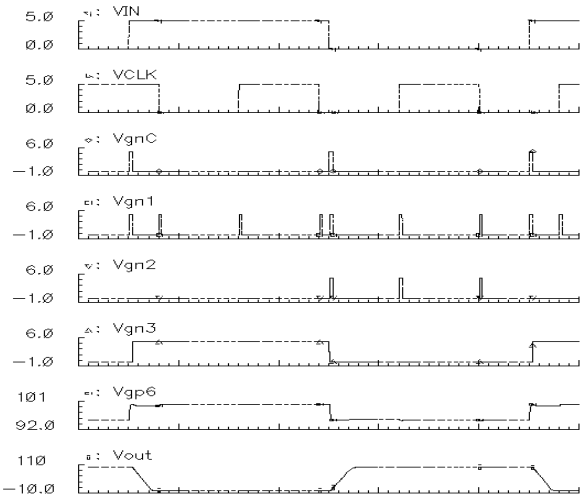


Fig. 4. Simulation results of the proposed circuit

Because gp6 is a dynamic node, a small subthreshold/leakage current from M_5 (V_{gs} of M_5 is about 0.5V-0.6V) and leakage current from M_2 will charge/discharge this dynamic node. This limits the minimum operating frequency of this level-up circuit. Signal V_{CLK} and gate I_{13} to I_{18} generate refresh control signals V_{gn1CLK} and V_{gn2CLK}, which are pulsed for a short duration τ_3 when V_{CLK} has a transition. V_{gn1CLK} and V_{gn2CLK} are passed to V_{gn1} and V_{gn2} for refresh operation when V_{gnC} is low.

From the above analysis, the level-up stage only conducts for a short duration τ_1 or τ_3, when input signal or clock signal make a transition, which significantly decreases the power dissipation of the level-up stage. On the other hand, output transistors M_3 and M_6 are never turned on at the same time, which minimizes the short-circuit power of the output stage. Simulation results show that the power of the level-up stage and short-circuit power of the output stage can be reduced to 5% of the total power consumption of the circuit (observed with a V_{pp}=300V, C_{load}=32pF test case, which is the load of an actual test probe setup).

III. DESIGN METHODOLOGY

A. Feedthrough From the Output Node

From simulations, we find that the V_{gp6} waveform has the following features: When V_{gn1} goes high, V_{gp6} is pulled up to

V_{pp} and M_6 is turned off, the output signal V_{out} decreases from V_{pp}. When V_{gn1} goes low, V_{gp6} has a voltage drop ΔV from V_{pp}, and this voltage drop mainly occurs when output transistor M_6 is in the triode region (Fig. 5b). In addition, ΔV depends on the value of capacitor C_1: the smaller the capacitor C_1, the bigger the voltage drop ΔV. If ΔV is too large, such as more than 0.8V (the threshold voltage of HV PDMOS), the output transistor M_6 will be turned on, thus causing short circuit current in the output stage.

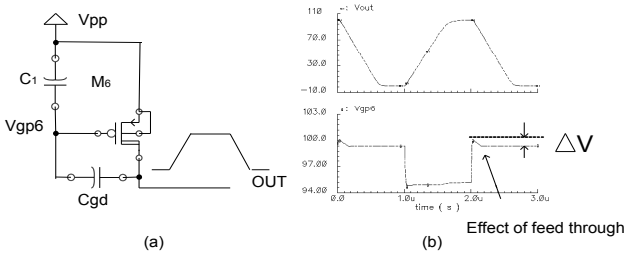


Fig. 5. Effects of feedthrough from the output node: (a)Principle (b) Waveform

This phenomenon is due to feedthrough from the output node. V_{gp6} is sensitive to the switching of the high voltage output node through the gate-drain Miller capacitance C_{gd} of HV PDMOS transistor M_6 (Fig. 5a). If we ignore the parasitic capacitance of node gp6, because of their small values, the voltage drop is shown in (1).

$$\Delta V = \frac{C_{gd}}{C_1 + C_{gd}} \Delta V_{out} \qquad (1)$$

C_{gd} is mainly due to the oxide capacitance when M_6 is in the triode region. Indeed, C_{gd} decreases significantly in the saturation region, because it is equal to a depletion capacitance in series with an oxide capacitance [6]. Therefore, ΔV mainly happens when M_6 is in triode region. From the I-V curve of HV PDMOS, we learn that $V_{ds\text{-}sat}$ is 20 Volts. We can use the above formula to find the minimum capacitance C_1. For example, to have $\Delta V<0.6V$ (the threshold voltage of HV PDMOS is 0.8V), we need $C_1 > 32.3C_{gd}$ (capacitance in the triode region).

B. The Timing of Control Signals

Special attention was paid to determine the timing requirements for safe operation as mismatches could lead to gate destruction by excess power dissipation.

Case 1: Timing requirements to ensure the "break before make" operation. The waveforms of some control signals due to an input rising edge are shown in the left part of Fig. 6. In order to avoid output transistors M_3 and M_6 turning on at the same time, we must respect the following relation:

$$t_r < \tau_1 \qquad (2)$$

For the input falling edges (right part of Fig. 6), we have:

$$t_5 < t_4. \qquad (3)$$

Case 2: Timing requirements between V_{gnC} and V_{gn1IN}/V_{gn2IN}. Signal V_{IN-} is used to disable V_{gn2IN}/V_{gn2CLK} when V_{IN} is high, and to enable V_{gn2IN}/V_{gn2CLK} when V_{IN} is

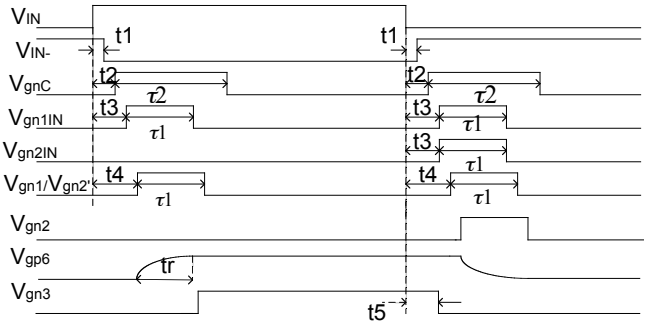


Fig. 6. Waveforms of the control signals

t_1: delay of I_9, t_2: delay of XNOR(I_{12}), t_3: delay of XNOR(I_4) and AND(I_5), t_4: t3+delay of MUX, t_5: delay of I_8, tr: rising time of V_{gp6}, τ_1 (delay of I_1 to I_3), τ_2 (delay of I_1 to I_3 and I_{10}, I_{11})

low. To ensure such enabling and disabling, we should have:

$$t_1 < t_2 \qquad (4)$$

In order to pass the complete V_{gn1IN}/V_{gn2IN} to V_{gn1}/V_{gn2}, pulses V_{gn1IN}/V_{gn2IN} should fit inside pulse V_{gnC}. This implies that we should have:

$$t_2 < t_3 \qquad (5)$$

$$\tau_1 < \tau_2 \qquad (6)$$

Case 3: Timing requirements between V_{gn1} and V_{gn2}. From the operation of this circuit, we know that, ideally, V_{gp6} is equal to $V_{pp} - 5V$ when the output transistor M_6 is turned on. In order to keep V_{gp6} at that value, M_5 and M_2 should be turned on/off at the same time. Considering the delay between V_{gn1} and V_{gp4_5} (V_{gp4_5} is shown in Fig. 3), the timing requirements of V_{gn1} and V_{gn2} are shown in Fig. 7.

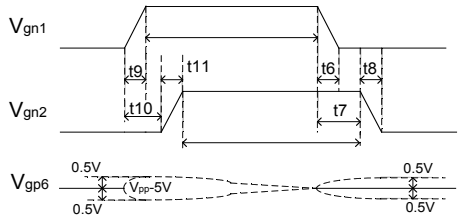
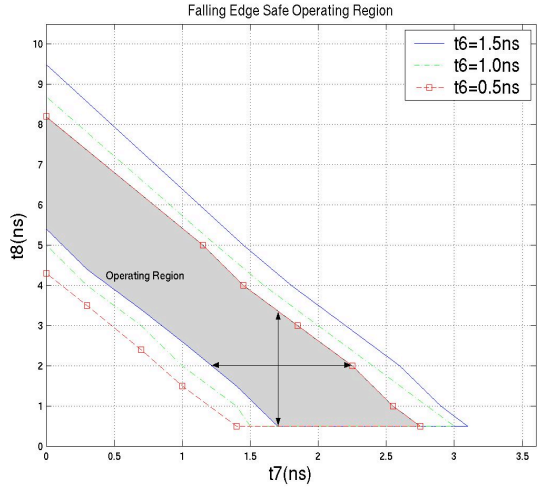


Fig. 7. Timing constraints between V_{gn1} and V_{gn2}.

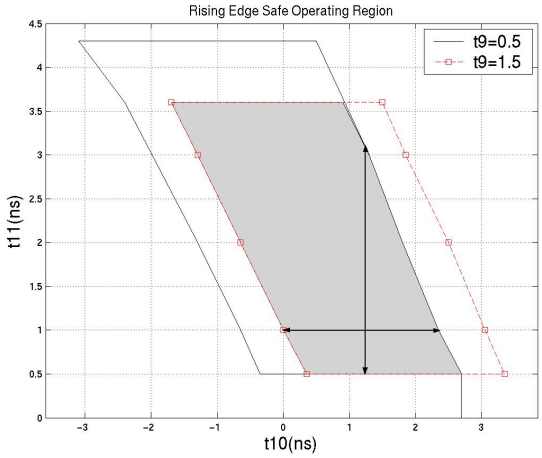
t_6: falling time of V_{gn1}, t_7: delay between V_{gn2} and V_{gn1}, t_8: Falling time of V_{gn2}. t_9: rising time of V_{gn1}, t_{10}: time shifting between rising edge of V_{gn2} and V_{gn1}, t_{11}: rising time of V_{gn2}.

Assuming 10% variation of V_{gp6} is acceptable, then we must have V_{pp}-5.5V<V_{gp6}<V_{pp}-4.5V. From simulations, the required falling edge timing parameters t_6, t_7 and t_8 are related as shown in Fig. 8a. (C_1=3p). The grey area defines a falling edge safe operating region (FESOR). We can design the circuit such that timing parameters t_6, t_7 and t_8 are in the FESOR. For example: 0.5ns<t_6<1.5ns, 1.2ns<t_7<2.25ns, 0.5ns<t_8<2.75ns (defined by the pair of arrows in fig. 8a). The relation between timing parameters associated to the rising edge t_9, t_{10} and t_{11} are shown in Fig. 8b. The grey area defines a rising edge safe operating region (RESOR). For example: 0.5ns<t_9<1.5ns, 0<t_{10}<2.35ns, 0.5ns<t_{11}<3.2ns (as defined by arrows in fig. 8b).

Case 4: Validation of asynchronous control circuit. The circuit could fail if the voltage drop of M_5 is large enough to exceed the gate-source breakdown voltage of M_6, or too



(a)

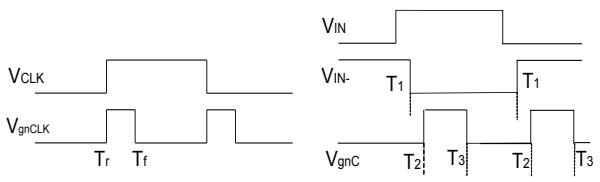


(b)

Fig. 8. Timing safe operating region
(a) FESOR (b) RESOR

small to turn on M_6. We should validate that the control signals V_{gn1} and V_{gn2} should fall in FESOR and RESOR for any phase relation of asynchronous input signals V_{IN} and V_{CLK}.

Our analysis of the safe operating region is related to the phase relationship between V_{IN} and V_{CLK}. Such relationship is represented as function of some timing parameters defined in Fig. 9 and that corresponded to some actual signals in the controller (V_{gnCLK}, V_{gnC}, and V_{IN}). Table 1 partitions the set of possible phase relationship based on those timing parameters. Detailed validation and simulation of all these conditions were conducted. It was found that safe operation is guaranteed in all regions.



(a) (b)

Fig 9. Some critical time:
(a)The time represented V_{CLK} (b) The time represented V_{IN}

Table. 1 Partition of required phase relationships
t_{12} is the delay of AND gate I_5/I_6 or I_{17}/I_{18}

V_{IN} falling edge		Condition	V_{IN} rising edge		Condition
$T_f<T_1$		no	$T_f<T_1$		no
$T_1<T_f<T_2$		$t_{12}>T_2-T_1$	$T_1<T_f<T_2$		$t_{12}>T_2-T_1$
$T_2<T_f<T_3$	$T_r<T_2$	$t_{12}>T_2-T_1$	$T_2<T_f<T_3$	$T_r<T_2$	$t_{12}>T_2-T_1$
	$T_r<T_2$	no		$T_r<T_2$	no
$T_3<T_f$	$T_r<T_2$	$t_{12}>T_2-T_1$	$T_3<T_f$	$T_r<T_2$	$t_{12}>T_2-T_1$
	$T_r>T_2$	no		$T_r>T_2$	no

IV. CONCLUSION

The high voltage level-up shifter presented in this paper reduces power consumption through dynamic operation and through the "break before make" concept. An asynchronous control circuit that refreshes a dynamic node was proposed to enable low frequency operation. A design method was proposed to ensure robust operation. It specifies required relationship between timing parameters that define a safe operating region, and it also allows selecting an appropriate value for a critical internal capacitor C_1 whose value is determined by feedthrough from the output signal. Simulation results show that the dynamic power for charging/discharging the load capacitance can be up to 95% of total power consumption of the circuit (V_{pp}=300V, C_{load}=32pF).

ACKNOWLEDGMENTS

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