Very Large Area CMOS Active-Pixel Sensor for Digital Radiography

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***Abstract*—To address the growing demand for low-noise large-area digital-radiography sensors, a unique CMOS active-pixel sensor (APS) technology has been developed. Large-tiled CMOS radiographic panels can compete in performance with passive-pixel arrays, amorphous-silicon thin-film-transistor panels, and phosphor-panel technologies. Although CMOS sensors have become a key technology in low-cost consumer camera products, CMOS APS technology is also suited for manufacture of large-format imagers used to construct radiographic-detector panels. Large-area CMOS radiographic sensors combine a large full well over 3.5 million $e-$ with low read noise less than 300 $e-$ to provide wide dynamic range and improved signal-to-noise ratio under demanding radiographic imaging conditions. With precision-assembly techniques, tiling gaps are minimized to be less than 0.3 pixels to produce fully correctable flat-field images. Applications include nondestructive testing, scientific imaging, security screening, and medical radiography.**

***Index Terms*—CMOS active pixel sensor (APS), digital radiography, dynamic range, large area, read noise, tiled array, X-ray imager.**

I. Introduction

FOR MORE than 100 years, radiological examinations were permanently recorded on film, and hence, the metrics for determining image quality and usefulness for a particular application have evolved around film-based technologies. Visible charge-coupled device (CCD) sensor technology has been successfully applied in some scientific and medical X-ray imaging applications by being integrated into image-intensifier systems or by affixing a tapered fiber-optic faceplate and scintillator to achieve a degree of magnification for a larger field of view. As amorphous-silicon (a-Si) thin-film-transistor (TFT) technology emerged in flat-panel-display applications, passive-pixel single-transistor radiographic-detector arrays were created using a-Si technology. Direct-coupled a-Si TFT arrays have been successfully fabricated on very large glass panels suitable for the large medical chest X-ray format. While a-Si TFT technology is versatile and manufacturable in large areas, it suffers from high read noise from combined pixel and line noise sources ($> 1000\ e-$) [1], pixel-pitch limitations, and resistance to lowering of manufacturing costs. CCD technology, while offering excellent low-noise performance, does not economically scale to larger imaging formats.

To address the limitations of currently established technologies, a very large area (VLA) CMOS active-pixel sensor (APS) technology has been developed for digital-radiography applications.

As the mainstream of CMOS IC applications drive silicon technologies toward the extremes of single-atomic-layer device engineering, an ingenious and valuable application for legacy CMOS foundry processes has been successfully exploited in the manufacture of VLA CMOS APSs for use in the growing market of digital radiography. The large active image areas required for radiography applications are realized by tiling multiple VLA sensors into a larger sensor panel. Image-sensor tiling was first reported in the late 1970s beginning with long CCD TDI detectors, and the tiling technology continued to develop through the 1980s and 1990s, principally applied to large CCD-based focal planes [2], [3]. Large-pixel tileable CMOS visible-detector technology is well suited for use in radiological-imaging applications because it is manufacturable in large areas, meets or surpasses radiological performance requirements, and offers digital-imaging system design flexibility not available from other radiological-imaging technologies.

Digital radiography relies on penetrating X-ray photons being transmitted through objects of interest and then being absorbed by down-converting phosphors such as gadolinium oxi-sulphide (Gd_2O_2S) or cesium iodide (CsI). The phosphors emit visible photons that generate photoelectrons collected and read out from an array of large p-n junction photodetectors. In the case of a CMOS APS, the electron charge is converted to voltage by a source–follower circuit coupled to each junction detector. To capture an image, the M $\times$ N array of pixel-voltage values is scanned in a parallel/serial sequence and output to analog-to-digital converter (ADC) circuitry for further signal processing before storage or display. The resultant density and thickness maps of targets placed between the X-ray source and the CMOS detector are studied in a multitude of applications, from printed-circuit-board inspection to dental CT. Each application of X-ray imaging technology has established parameters unique to that application, and digital-imaging systems are often tailored to provide optimal radiological performance for major application markets.

With a few exceptions, digital X-ray imaging systems do not utilize lens optics, and system resolution is defined, to first order, by the X-ray source spot size. Except for systems that use microfocus (and recently nanofocus) X-ray sources, the X-ray source spot sizes for most applications are relatively

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large ($> 50\ \mu$m), resulting in successful use of image-sensor technologies that can be manufactured in large areas, without being forced to use advanced process technologies for fine-pitch feature sizes.

Digital X-ray imaging systems are largely defined by their active detector area. Since X-ray imaging technology mostly relies on a 1 : 1 aspect ratio, coverage area tends to define the applications and markets for various classes of imaging technologies. Medical applications such as chest X-ray require large detector active areas (≥ 43 cm $\times$ 43 cm) and relatively low resolution (< 4 lp/mm), while intraoral dental sensors are confined to sizes of 20–40 mm per side with smaller pixel pitch ($< 25\ \mu$m). Inspection of printed circuit boards can be accomplished using 5 cm $\times$ 5 cm detectors while mammography applications require active areas as large as 25 cm $\times$ 30 cm. It is therefore challenging to develop a sensor technology that meets multiple-imaging requirements that can also be scaled to different sizes of active area. The tileable CMOS APS technology achieves the desired resolution, dynamic range, scalability, and cost figures of merit for a broad range of digital X-ray imaging applications.

In 2000, a manufacturable radiographic CMOS array technology was developed by Graeve and Weckler [4] that utilized an innovative tileable CMOS APS sensor design, featuring a 48-μm pixel pitch, 512 $\times$ 1024 array resolution, a 2.5 cm$\times$5 cm active area, 2.3 million $e-$ full well, and less than 150 $e-$ read noise. The VLA sensor described in this paper has its origins in the earlier sensor design. To create panels with larger active area suitable for mammography and other medium-sized coverage applications, the high-resolution CMOS array has been scaled up to a tileable 96-μm APS technology, using the same array format (512 $\times$ 1024 pixels), but a 5 cm $\times$ 10 cm active area. Eight tiled VLA sensors have been assembled into 20 cm $\times$ 20 cm panels with 2048 $\times$ 2048 pixels and 5-lp/mm resolution [5]. Ultimately, the technology can be used to create panels up to 20 cm $\times$ 30 cm to address applications ranging from nondestructive testing (NDT) to medical radiography.

Design and performance characteristics of VLA, three-side-tileable CMOS active-pixel image sensors will be discussed. Tiled-panel technology, including sensor architecture for close tiling and X-ray detector module construction, is presented.

Future developments in VLA sensor and large-area tiled X-ray detector technologies will address performance improvements such as frame rate, improved pixel response, further noise reduction, and larger active areas. The sensor improvements will address requirements of scientific and medical applications which most often determine the performance-improvement standards for detector technologies.

II. Sensor Architecture

Fig. 1 shows the three-side-tileable VLA CMOS sensor floor plan that enables close tiling for construction of large radiographic panels. The pixel pitch is 96 μm, with an active area of 49.1 mm $\times$ 98.3 mm. On-chip CMOS circuitry includes bias conditioning, control logic, clock drivers, a row address register, column amplifiers, a column scan register, and output circuits. Sensor tiling requires placement of the row address register in the center of the array, where it occupies an active area equivalent to 1.5 columns. Pixels adjacent to the address register are scaled accordingly to retain the integer pixel spacing. On three sides of the sensor, the active-pixel area is placed as close to the die edge (scribe line) as possible. The gap between edge pixels on adjacent tiled sensors typically occupies between 1.0 and 1.5 pixels, which again can be compensated by scaling the edge pixels to a narrower width. A photo of the assembled VLA CMOS sensor is shown in Fig. 2.

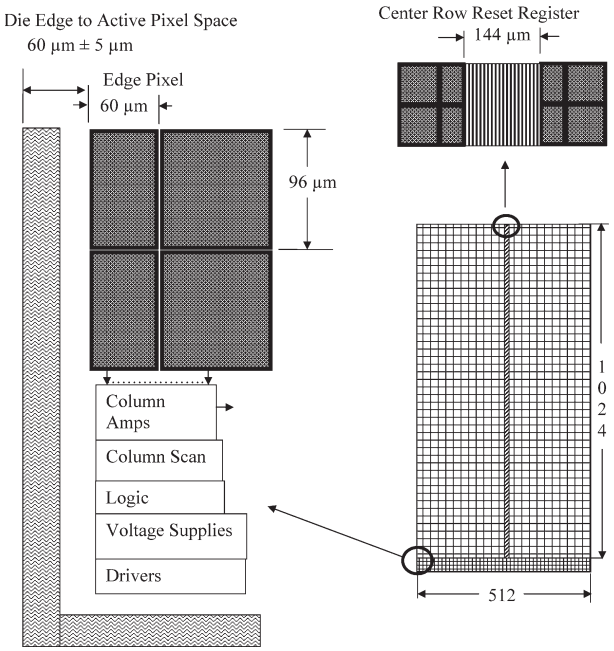

Fig. 1. VLA CMOS sensor die ayout.

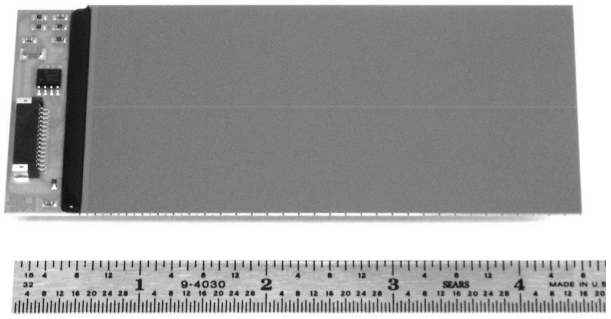

Fig. 2. Assembled VLA CMOS image sensor.

Fig. 3 shows the profile of an assembled sensor panel constructed by tiling VLA CMOS sensors together. The stack consists of a module housing, a metallized ceramic substrate upon which the CMOS sensor has been die attached and bonded, an optional fiber-optic faceplate, a scintillator film, a foam-compression layer, and an optically opaque cover plate that has low X-ray absorption. The tiled sensors are aligned to within 10 μm (≤ 0.1 pixel) in both x- and y-directions and leveled to maintain a flat image surface. As an efficient absorber of X-ray radiation, the fiber-optic faceplate prevents direct absorption of X-ray photons in the CMOS detector, leading to a lower noise

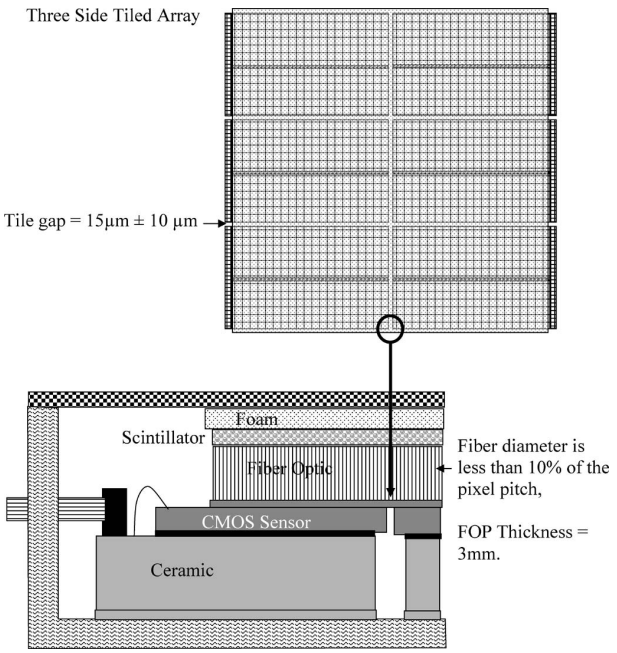

Fig. 3. Cross section of an assembled VLA CMOS X-ray panel.

power spectrum and consequently improved detective quantum efficiency at high spatial frequencies [6].

With a tiled digital X-ray panel application as the primary design driver for the VLA CMOS sensor, special attention is paid to several specific architectural features: 1) Pixel size is driven by the radiological application, X-ray source spot size, and manufacturing yield potential. Small pixels are not necessary and not desirable because a large full-well capacity is more desirable for dynamic range, and the majority of applications do not require an imaging system with resolution better than 2–10 lp/mm. Large pixels allow for a less dense layout of critical layers such as metal lines, which impacts yield and ultimately cost. 2) Except for fluoroscopy and CT applications, few systems require frame rates in excess of a few frames per second. The VLA circuit is designed to operate with master clock frequencies of 1–2 MHz. Large parasitic capacitance and long metal bus runs will limit high-speed clock performance. Consideration is given to worst case clock waveforms and clock edge delays to avoid waveform-propagation issues. 3) Pixel-layout parameters, particularly the photodiode layout, are tailored to optimize charge-to-voltage conversion efficiency and QE*ff (quantum efficiency times fill factor), while minimizing reset-level variation (kTC) read noise. Adding circuit elements to achieve better or more versatile pixel performance, such as in-pixel correlated double-sampling (CDS) to reduce read noise, results in adding circuit complexity which reduces yield and increases cost. Unlike visible-imaging applications, small gains in signal-to-noise performance are not the primary drivers for most radiographic applications where X-ray photon shot noise is the limiting noise performance factor. The VLA sensor does contain circuitry to correct for fixed-pattern offsets from pixel and column transistors. However, this type of correction affects spatial nonuniformities only and does not correct for temporally correlated noise sources.

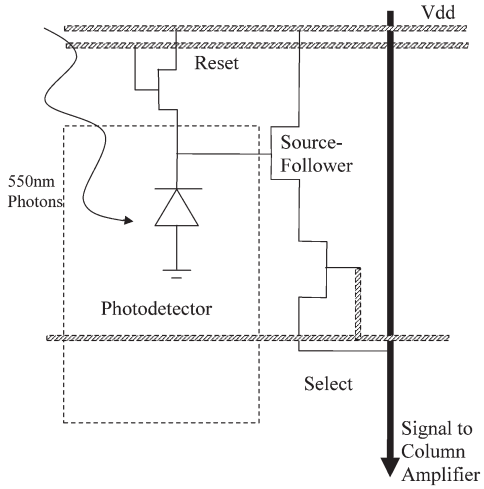

Fig. 4. Pixel circuit detail.

III. Pixel Design

Fig. 4 shows the VLA CMOS image-sensor pixel circuit. Design and layout simplicity are critical, with a basic three-transistor (3T) CMOS APS pixel structure being preferred to more complex structures such as 4T, 5T, and larger transistor count pixels. Early sensor design experiments have revealed that large-area large-pixel CMOS sensors do not benefit from snapshot or global shutter circuits in most applications. From early work on photodiode-array technology [7]–[9], it can be inferred that, for a given process technology, large-pixel CMOS APS sensors produce an analog responsivity that is largely independent of pixel size. This is the case because, as the photosensitive aperture increases or decreases with pixel pitch, the sense-node capacitance, and therefore the conversion gain, also increases or decreases proportionally. As long as the sense-node capacitance and the pixel aperture scale together, the signal level will remain relatively constant for a given light level. This is true because

$$S = I \times QE \times ff \times G \times A \tag{1}$$

where I is the photon flux per unit area, $QE \times ff$ is the internal quantum efficiency of the photodiode detector times the percentage of optically clear aperture per pixel, A is the pixel area, and G is the conversion gain of the pixel circuit. G can be expressed as

$$G = g \times \gamma \tag{2}$$

where g is the source follow gain (0.7–0.8 per stage) and γ is the charge-to-voltage conversion efficiency of the sense node. The conversion efficiency γ is a function of the sense-node capacitance expressed as

$$\gamma = q_e / C_{\text{node}}. \tag{3}$$

Since C_{node} for large pixels is primarily a function of the junction capacitance (area and periphery) of the photodiode—assuming the reset/source–follower FET and source/drain

dimensions remain small and constant for scaling purposes—the ratio of the pixel signal for two different sizes of pixel is

$$S_1/S_2 \cong A_1 \times \gamma_1/A_2 \times \gamma_2 = A_1 \times C_{\mathrm{node2}}/A_2 \times C_{\mathrm{node1}} \tag{4}$$

assuming QE and ff are essentially the same in both cases. To first order, and considering that the reset and source–follower FETs and parasitic capacitances on the sense node are small, C_{node} can be estimated from the photodiode junction area and periphery as

$$C_{\mathrm{node}} = C' \times A_d + C'' \times P_d \tag{5}$$

where C' is the process value of capacitance per unit area, C'' is the process value of capacitance per linear junction, and A_d and P_d are the area and periphery junction dimensions. It can be argued, for the sake of approximation, that the junction area and periphery values used for calculating the node capacitance scale linearly for large pixels for simple expansion or shrinkage of the pixel (i.e., the photodiode proportion of the pixel is invariant) such that

$$C_{\mathrm{node1}}/A_1 \cong C_{\mathrm{node2}}/A_2 \tag{6}$$

and therefore

$$S_1/S_2 \cong A_1 \times A_2/A_2 \times A_1 = 1. \tag{7}$$

It is this principle that allows for the design of partial pixels to be used at the borders of the row register feature to "fill in" columns with approximately the same responsivity as the normal columns with the full-pixel pitch. For the device described in this paper, the edge and center pixels are 60 μm wide by 96 μm high. The aperture is 60% of the full-pixel aperture, and the photodiode capacitance is adjusted to be 60% of the full-pixel capacitance, such that the charge to voltage conversion gain is 40% higher than the full-sized pixel. Flat-field imaging data confirm that the edge-pixel response is within 5% of the full-pixel response. This principle works well for pixel pitch larger than approximately 30 μm. For smaller pixel pitch, the percentage of the active pixel used for the reset and source–follower circuits becomes large enough to affect the scaling assumptions.

IV. CMOS Circuitry

The VLA CMOS sensor is scanned in a row-sequential "rolling shutter" readout sequence, where the photodiodes in each row are sampled and reset in parallel. A row address register is used to generate the select and reset signals for each row. As a particular row of pixels is selected, the voltage from each photodiode is transferred onto a column bus or column data line, with a current source located at the bottom of the array completing the source–follower amplifier circuit. The output voltage of the pixel source–follower is stored in one or more sample-and-hold capacitors, which can then be scanned sequentially to complete the readout sequence. Fig. 5 shows this concept.

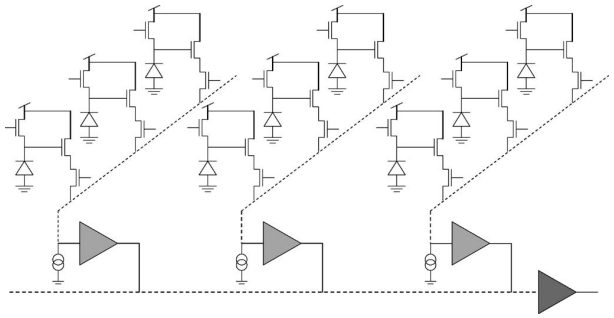

Fig. 5. Column readout circuit schematic.

The sensor also features a nondestructive-readout (NDR) mode in which the signal voltages from each row of pixels are sampled, but the pixels are not reset in the process (i.e., the reset signal from the row address register is suppressed). The NDR mode allows for acquiring a snapshot of the image at various times while signal is continuously accumulating. Typical applications for this type of readout are an autoexposure mode, where the exposure is checked at regular intervals to determine the optimum exposure time, and a low-noise readout mode, where the signal is determined by subtracting two successive nondestructively read image frames. Because the pixel capacitance is not reset in this mode, this scheme effectively subtracts out the pixel reset (kTC) noise, which tends to be the dominant noise source in the VLA sensor.

Additionally, the VLA sensor can also be operated in a sparse-sampling readout mode, where odd-numbered rows and even-numbered columns are skipped during the readout sequence. This allows a low-resolution scan of the image in roughly 1/4 the time required to read out the full image. Sparse sampling is useful for applications requiring a temporary switching to a video mode, while stationary images are acquired at full resolution. For the sparse sampling to be effective, the circuit design enables periodic resetting of the unused pixels; otherwise, the unsampled photodiodes soon saturate. As a result, unwanted signal electrons will drift into adjacent pixels, leading to unpredictable nonlinear blooming effects. In the VLA sensor, the unused rows are still reset during the horizontal blanking interval, even though the collected signal is discarded during the readout.

V. Device Performance

The VLA CMOS sensor is a visible imager, and Fig. 6 shows the measured spectral response of the device using light-emitting diodes (LEDs) for narrowband illumination. At 550 nm, the measured QE*ff is 47% $\pm$ 3%. The photodiode junction depth and depletion region resulting from the CMOS foundry process are sufficient to capture a significant percentage of the electrons generated by the 550-nm photons emitted from the scintillator. The QE*ff is also affected by internal diode drain structures which border the pixel active area. No microlenses are required as the open aperture of the pixel is $> 85\%$. The conversion gain of the pixel was measured using the mean variance method [10] with an LED light source at a wavelength of 550 nm providing illumination. The

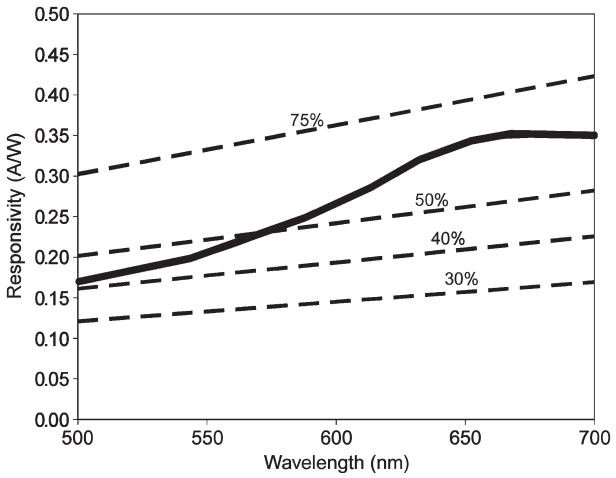

Fig. 6. VLA CMOS pixel spectral response. The dark line shows QE*ff for the VLA pixel. The dashed lines depict different QE levels at 100% fill factor.

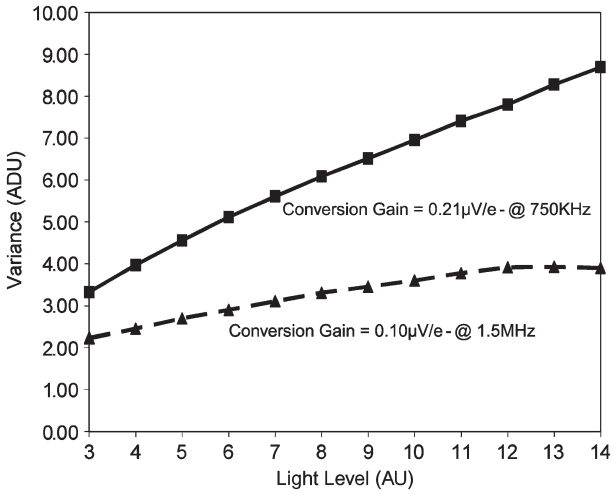

Fig. 7. Signal variance study. The pixel conversion gain is equal to the slope of the signal variance versus the mean signal, in [ADU/e-].

conversion-gain measurement was affected by the master clock frequency due to parasitic loads on the output register, changing the sampling point of the pixel output waveform. Slower clock frequencies provided more time for the analog waveform to reach full value prior to sampling. Fig. 7 shows measurements of signal variance for different operating frequencies. A 750 kHz clock rate enables a 1.3 fps data rate for large-area tiled panels, at a conversion gain of 0.21 $\mu V/e-$.

Dark current has been measured at various temperatures and follows the standard silicon diode leakage doubling rate statistics. At room temperature, the average dark current is 23 500 $e-/s$ with a corresponding rms noise of 153 $e-/s$. Fig. 8 shows a histogram plot of a typical dark-current distribution at room temperature. The dark signal nonuniformity is 8%, and the room-temperature dark-current density is 0.41 pA/mm^2 in early versions of the detector design. Later designs with improvements in surface trap stabilization demonstrate dark-current density of 0.33 pA/mm^2. For comparison,

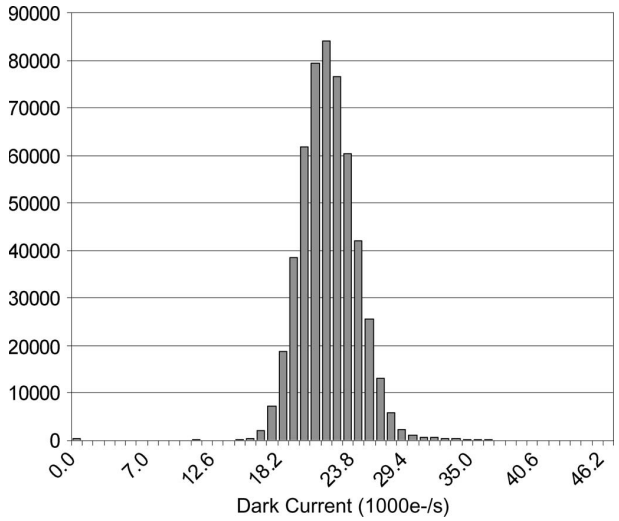

Fig. 8. Dark-current histogram. The mean dark-current value at room temperature is 23 500 $e-/s$, with a standard variation of 3000 $e-/s$.

recent investigations by Du *et al.* [11] on the characteristics of HgI detector materials applied to TFT pixels in test arrays report dark current less than 1 up to 23 pA/mm^2, depending on the method of processing of the HgI detector layer. Earlier reports by Kim *et al.* [12] indicate dark-current density for typical amorphous-silicon detector panels to be 2 pA/mm^2.

An accurate measurement of read noise (kTC) generated in the pixel is difficult to accomplish without developing custom low-noise test systems. In this paper, the total noise was measured using a low-noise camera electronics system with 14-b digitization. The dark-current shot noise in the sensor was reduced through cooling, by using short integration times, and by using the NDR method of subtracting frames of dark signal. The VLA CMOS sensor allows the NDR mode to be established with variable integration times. Successive frames of pixel dark signals are subtracted for several integration times, and the variance of the subtracted signals is calculated. The resulting value has an rms sum of dark leakage shot noise, kTC noise, quantization noise, and noise from the circuit-board Vdd and ground supplies. The total noise measured after cooling of the sensor and applying the NDR methodology has been measured at 580 $e-$ with a dark shot-noise component of 80 $e-$. Together, the quantization noise ($\sim$100 $e-$) and dark-current shot noise are negligible as compared to the camera board noise floor estimated at $\sim$500 $e-$. As it is not practical to further reduce the noise generated by the power supplies and because the quantization noise is fixed by the 14-b ADC, the noise figure for reset kTC must be estimated to be greater than 200 $e-$ but less than 400 $e-$. From the node-capacitance calculations for the pixel, the theoretical value of the kTC noise is expected to be 250 $e-$.

The calculated full-well charge capacity for the VLA CMOS pixel using a 5-V reset supply is 11 600 000 $e-$, based solely on the total capacitance of the photodiode and parasitic capacitances of the detector node and a well depth of 5 V. However, not all of this charge capacity is accessible, since transistor thresholds in the readout circuitry limit the usable voltage swing

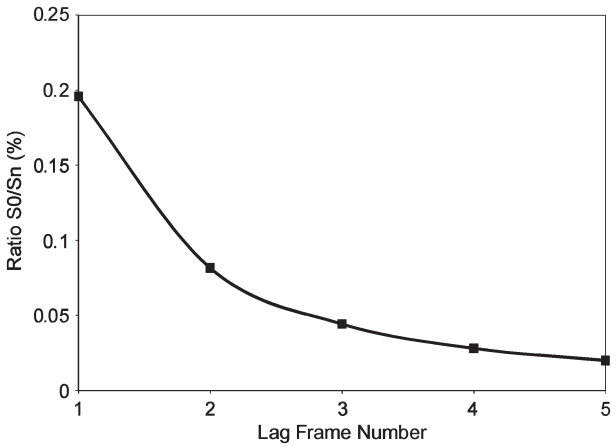

Fig. 9. Study of remnant signal (image lag) in the VLA CMOS pixel. The light source is a pulsed LED at 550 nm, the readout speed 5 ft/s.

TABLE I
VLA CMOS PERFORMANCE SPECIFICATIONS

Specifications	*Typical*	*Units*
Avg. dark current (at 21°C)	23,500	electrons/sec
Read noise (rms, at 1 fps)	250	electrons
Saturation	4,500,000	electrons
Dynamic range	85	dB
Frame rate	1.3	fps
Data rate (CLOCK)	750	kHz
Conversion gain	0.21	μV/electron
Response linearity (average)	± 1	% of sat.
Quantum Eff. (QE*ff @ 550 nm)	45	%
Image Lag (at 1 fps)	<0.05	%
Supply voltage (VDD)	5.0	V
Supply current (IDD)	30	mA
Power Dissipation	<200	mW

on the pixel node to less than half of the supply voltage. In the present pixel design, a "hard reset" is employed. At small signal levels the 3T pixel circuit exhibits a non-linear response of output voltage versus pixel input voltage, the causes of which are under investigation. The investigation includes study of the row select, as well as the source-follower and reset MOSFET characteristics, at conditions where the input voltage to the source-follower approaches Vdd.

The effects of the small signal nonlinearity on imaging performance will be discussed in depth in a subsequent paper. Large-signal response linearity is limited by the changing depletion capacitance as the large-signal charge moderates the depletion region of the detector photodiode. The useful linear range of the sensor is limited by camera dc-offset adjustments to approximately 0.8 V at the output corresponding to 3 810 000 $e-$. The maximum dynamic range of the VLA CMOS sensor, using the expected value for kTC read noise of 250 $e-$, is $20^{*}\log(\mathrm{N_{max}}/\mathrm{N_{noise}}) = 85.1$ dB. The useful linear dynamic range is 83.7 dB.

Image lag was measured by using a pulsed LED visible light source and operating at the maximum frame rate to observe the signal level in the illuminated pixels in frames subsequent to the initially integrated output from the pulsed source. Residual charge not removed from the pixel during the reset operation would be recorded in subsequent frames. Fig. 9 shows the decay of the remnant charge in the pixel. After 200 ms, the signal level is less than 0.2% in the first trailing frame and falls to less than 0.05% after three trailing frames. Except for fluoroscopy applications or high-frame-rate applications such as CT imaging, image lag in digital X-ray systems is seldom a concern.

The bulk of the power dissipated in the VLA CMOS sensor results from the dc currents supplying the biasing circuits. The relatively low master clock frequency and low duty cycles used in the VLA sensor design require little ac current. The sensor dissipates less than 150 mW at 5-V Vdd, such that a panel of eight VLA sensors will dissipate less than 1.2 W of power over 400 cm^2 of silicon area. Table I summarizes the performance of the VLA CMOS image sensor as a visible detector at the conditions nominally used to operate a tiled 20 cm $\times$ 20 cm digital-radiography camera.

VI. DIGITAL-RADIOGRAPHY APPLICATION

The VLA CMOS image sensor has been designed to accommodate a broad spectrum of radiological-imaging applications, including medical tissue biopsy, dental CT, industrial NDT, and X-ray crystallography. Each application requires emphasis on different performance features. Low dose and small signals are required in some applications, while high X-ray energies and high-dose rates are required in others. Making use of the full extent of a wide dynamic range is necessary in some applications. The VLA CMOS sensor has fixed performance features for responsivity, noise, and other process-related silicon detector parameters. The VLA sensor offers the option of increasing the frame rate by implementing the sparse sampling mode. Radiological performance can be adjusted through the optimization of scintillator materials, light-blocking windows, camera gain, and sensor cooling. If an application has limited photon flux, a scintillator with higher conversion efficiency will be used.

X-ray absorption is a function of the total amount of absorbing material, so that higher absorption efficiency for the typical GdOS scintillators requires thicker material layers of scintillator. The resolution of the X-ray camera is dependent on several factors, thickness of scintillator being one, due to the isotropic spreading of visible photons in the scintillator material [13]. Fig. 10 shows the MTF performance of a VLA CMOS sensor using two typical GdOS scintillator films. The Kodak Min-R 2190 film is capable of enabling a contrast of 20% at the theoretical Nyquist limit of 5 lp/mm. A thicker scintillator, such as DRZ Standard or Lanex Fast, is capable of absorbing a larger fraction of X-ray photons, hence resulting in increased camera sensitivity while suffering from a loss of resolution. The VLA CMOS sensor with DRZ Standard produces a resolution of 20% modulation at 2.7 lp/mm and less than 5% at 5 lp/mm. Fig. 11 shows a plot of the camera response to X-ray radiation at 50 kVp for these scintillators. MTF measurements were performed using a precision-machined tungsten edge and custom

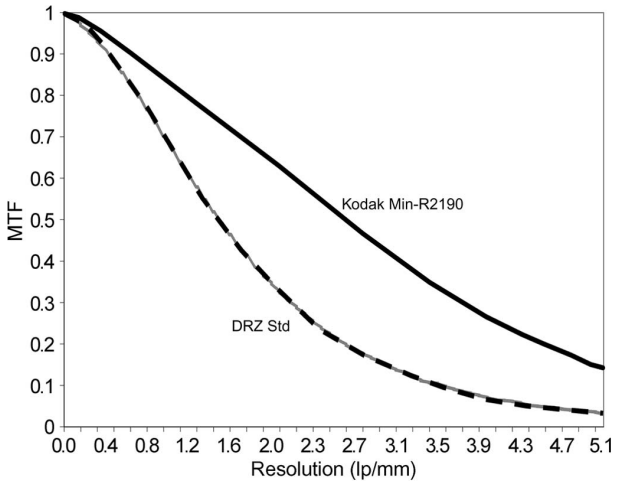

Fig. 10. VLA CMOS MTF for two scintillators.

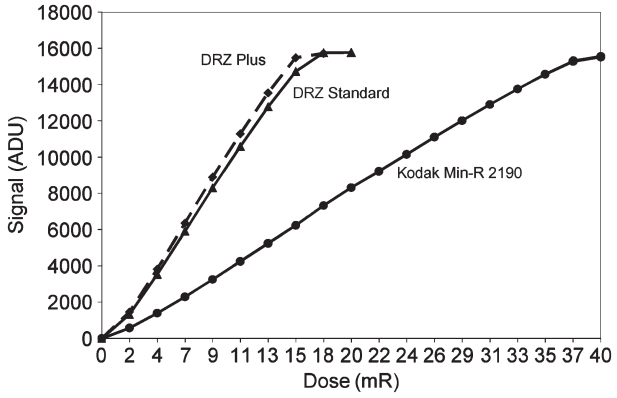

Fig. 11. VLA CMOS X-ray camera response.

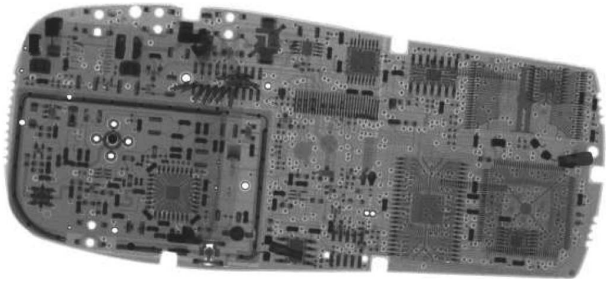

Fig. 12. Radiograph of a cell phone PCB across three VLA CMOS tiles.

Fig. 13. Radiograph of a Sandab across three VLA CMOS tiles.

software to calculate the sensor MTF from the edge response recorded in the image frame [14], [15].

Custom image-processing software is used to remove the dark-current signal by subtracting an averaged dark signal frame (dark offset) from each frame of data. Similarly, variations in the pixel response are removed by averaging several frames of flat-field image data and applying gain-correction algorithms to normalize the individual pixel response. This two-point correction is sufficient to remove most sensor-caused artifacts from the final application image. In special cases, more complicated nonlinear or piecewise-linear multipoint correction methods can be employed to completely remove variations in the detector response linearity from the image.

It is not possible to eliminate particulate and masking defects in the typical CMOS foundry process. Many types of process defects can be anticipated and mitigated through intelligent layout practices. The defects that result in shorting of metal lines usually cause single row or column outages due to disconnection of a bus line or shorting of a bus line to an unrelated signal line. Single, and even multiple, columns and rows that are nonresponsive may be corrected in a final digital image by mapping the pixel outages and applying a substitution algorithm to estimate the missing image content from neighboring pixels. Using a pixel map and substitution, digital radiographs will be rendered free of image defects. Data missing in the nonoperative pixels are generally nonessential as radiological-image features are rarely smaller than a few pixels. However, clusters of defective pixels and multiple adjacent row or column outages present a more difficult problem for pixel substitution. Simple two-point correction algorithms perform well with single pixel, row, and column defects, but more sophisticated algorithms are needed to correct larger defects [16]. Gain corrections are typically stable over time and from sensor to sensor. Frequent dark-current offset corrections are useful to insure calibration with regard to changes in operating temperature.

Figs. 12 and 13 show the quality of radiological images available from a tiled VLA CMOS digital panel. In both images, the target object spans three tiled sensor segments. Dark-current offset, gain normalization, and pixel corrections have been applied. Some minor image artifacts are visible due to nonoptimal defect correction resulting from nonoptimized operating conditions for a first prototype large-area panel; these types of defects are fully correctable in production devices. Fig. 12 shows an industrial NDT application requiring detection of broken traces, soldering defects, incomplete etch, etc., on fine-geometry printed circuit boards. Fig. 13 shows features in a biological sample requiring high-contrast signal-to-noise ratio

to locate small defects that have small density variation or, in the case of a medical application, lesions, fractures, and foreign matter. As an example of the excellent small-contrast signal-to-noise ratio obtainable from the VLA CMOS sensor, the image shown in Fig. 13 of the skeletal features of the fish depict easily discernable contrast between the soft tissue and the denser bone structures. This is true even though the signal contrast between the bone and the surrounding biomass is only 1.09 : 1.

VII. Conclusion

The VLA CMOS sensor reported in this paper moves the tiled CMOS array technology forward into the realm of large flat-panel applications such as mammography. Tiled panels of VLA CMOS sensors can be scaled to 20 cm $\times$ 30 cm and larger active areas and, combined with appropriate scintillator materials, will produce low-noise high-image-quality digital radiographs for medical, dental, industrial, and scientific applications. Future designs of VLA CMOS sensors will provide higher frame rates through multiple output taps and improved circuit performance. Fluoroscopy applications, as well as CT and other "real-time" or low-dose X-ray imaging applications, will drive the sensor and panel performance to higher frame rates. The VLA CMOS technology will be improved by reduction of read noise, particularly kTC noise, which can be accomplished through addition of CDS circuitry and NDR options. Radiation tolerance, particularly for higher X-ray energies, may be achieved through both external application of X-ray absorbing materials, such as fiber-optic faceplates, as well as CMOS design and process improvements.

As standard CMOS technologies evolve and mature, opportunities to cost-effectively apply large-area CMOS APS technology have materialized. Because pixel size in the digital X-ray application is not driven by consumer electronics market forces, more mature (> 0.35 μm) and less expensive CMOS technologies (150-mm wafers) can be successfully utilized to build large-area active-pixel arrays that will yield adequately, can enjoy higher voltage margins (5 V), and can be tiled into arrays as large as 20 cm $\times$ 30 cm. The advantages of lower read noise (< 300 $e-$), large full well ($> 3\,500\,000$ $e-$), full CMOS circuit design flexibility, low dark current, three-side tileability, and lower manufacturing cost enable the VLA CMOS X-ray sensor to be competitive in small- (< 10 cm $\times$ 10 cm) and medium (< 30 cm $\times$ 30 cm)-panel-size applications. Tiling of larger die and alternate tiling strategies will ultimately result in panels capable of satisfying even the largest medical radiography applications.

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