A CMOS High-Voltage DC-DC Up Converter Dedicated for Ultrasonic Applications

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ABSTRACT- This paper concerns the design and implementation of a fully integrated High Voltage CMOS DC-DC Up Converter (VHVUC) dedicated to ultrasonic transmitters. This VHVUC new topology, followed by a drive amplifier, is based on a multiple-stage charge pump circuit and a level-up Shifter is used in each stage as a clock generator in order to increase exponentially the DC voltage. A drive amplifier, based on a level-up stage and a class D switching output stage. It is used to excite the ultrasonic transducer, resonate at 3.5 MHz. Simulation results of the proposed converter, using a 0.8µm CMOS/DMOS High-Voltage process technology, show output voltage of 200 V with 83% gain voltage factor and a 95 mV output ripples for 2 MHz frequency. Also, the drive amplifier for single shock excitation show a 140 V spike at the transducer element with a pulse repetition time of 260µs and a rise and fall times of 220 ns and 713 ns respectively with a peak current through the transducer element of 25 mA. These results show the feasibility of applying HV process technology to replace conventional electronic transmitter technology.

I. INTRODUCTION

Medical ultrasound is used routinely in most hospitals for diagnosing soft tissue structures. The advantages of the technique are its lowest cost, real-time image formation, mobility, noninvasive nature, and no known bioeffects in the used frequency range [1]. The miniaturization of such ultrasonic systems provide low power dissipation, good bulk, and low weight [2].

In diagnostic ultrasonic applications, DC level higher or equal to 200 Volts must be applied to reach a large depth in human body [3]. To generate the required high DC voltage, several circuits were designed. Some of those are based on coupled-inductor to achieve the high voltage gain [4], others based on capacitor chains, which are interconnected by diodes and coupled in parallel with two non-overlapping clocks [5]. Also, electromagnetic transformers were designed to generate the required high voltage [6]. However, all of the previous designs are made on PCBs using discrete components.

We propose in this paper a fully integrated HVCMOS DC-DC converter followed by a drive amplifier dedicated to drive MEMS based ultrasound cells. This system on chip (SoC) device is intended to build a hand-held ultrasonic system.

Section II presents the design of the fully integrated VHVUC. Drive amplifier is reported in section III. The simulation results are shown in section IV, and conclusions are the subject of section V.

II. DESIGN OF THE VHVUC

The block diagram of the VHVUC, based on a 5-stage voltage doubler, is shown in figure 1. A level-up Shifter is used in each stage as a clock generator in order to increase exponentially the voltage. By cascading n voltage-doublers, the output voltage of the btained VHVUC can be expressed as follows :

$$V_{out} = 2^{n-1}\left(V_{in} + V_{clk}\right) \quad (1)$$

where V_{in} and V_{clk} are the amplitude of the input and the clock signals respectively and n is the number of stages.

Each stage consists of a voltage doubler circuit, a voltage level up Shifter and a level up stage. The voltage doubler circuit shown in figure 2 is composed of a cross-connected HVNMOS transistors M_1-M_2 and the pair HVPMOS transistors M_3-M_4 used, as serial diode, to transfer the charge from one stage to the next. Two phase non-overlapping clocks CK_1, CK_2 are used to drive the pumping capacitors (C_1, C_2) of each stage. In the voltage doubler circuit, the use of the N-type transistors improves the performance of the charge pumping due to its faster carriers (electrons versus holes), smaller size and less parasitic capacitors. Its threshold voltage (V_T) causes a problem for low voltage application, but for high voltage, this problem is avoided.

By using a faster configuration of cross-coupled HVNMOS transistors with fast operating clock frequency and less parasitic capacitors improves the gain voltage of each stage. This configuration leads to an automatic reverse biasing of the parasitic bipolar transistors (lateral, vertical) [7].

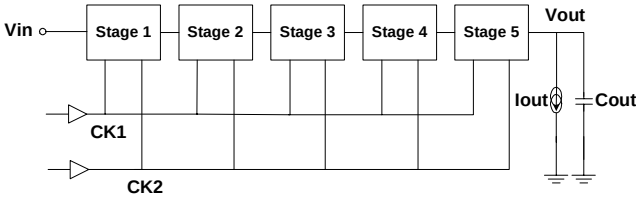

Fig. 1 Simplified block diagram of the proposed DC-DC up converter

A. Technology process

Today the Double Diffused Metal Oxide Semiconductor (DMOS) transistor has become the primary choise for high-voltage integrated circuits. By employing RESURF techniques, it is possible to combine low-voltage (LV) standard CMOS logic with high-voltage (HV) output stages where the voltage switching capability exceeding 400V [8]. The adopted process for the present work is the 0.8µm 5V/HV CMOS/DMOS process (with three metal layers) triple wells provided by DALSA Semiconductor. This smart process consists of modifiying a low-voltage CMOS technology to accommodate a high-voltage option. High-voltage capability is obtained when combining the existing technological layers in an unconventional way in order to create low concentration doping regions. Cross-section of n- and

p-channel HV-devices are given in figure 3. The HV NDMOS transistor has the source and channel regions, including the thin gate oxide, identical to those of standard NMOSs. Its V_T and transconductance are controlled by the same parameters as the NMOSs.

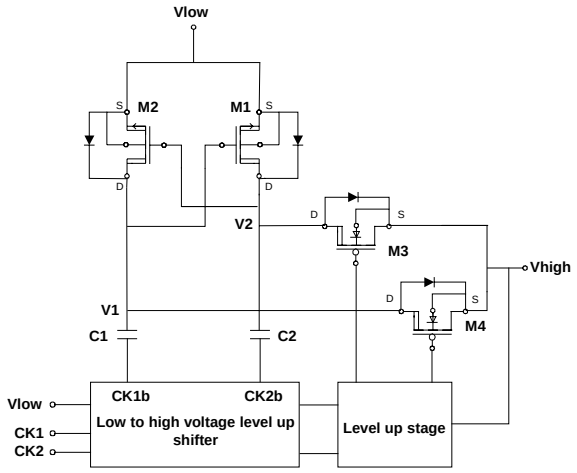

Fig. 2 Schematic of one stage voltage doubler circuit

However, in order to withstand high drain-to-source voltage (V_{DS}), the drain is separated from the edge of the channel P-base by a lightly doped P-drift and buffer region formed by the HVN-Well implant. It is important to note that, since the gate oxide is the same as that of standard LV devices, the maximum V_{GS} cannot exceed 10V. For the HV PMOS transistor, the drain is separated from the edge of the channel HVN-Well by a low doping concentration P-drift region in order to withstand high V_{DS}. The DALSA process has two types of HVNMOS devices. The high side floating source which is connected to its local bulk and can withstand 100V and its Breakdown (BV_{DS}) is ≤ 120V. The other type is the low side one and its source is also connected to its local bulk which is connected to P-sub and can withstand few volts and its BV is ≤ 300V. The source-drain BV for HVPMOS is ≤ 400V. It is important to note that when the bulk-source voltage (V_{BS}) is 0V for HV transistors, they have a unidirectional functionality.

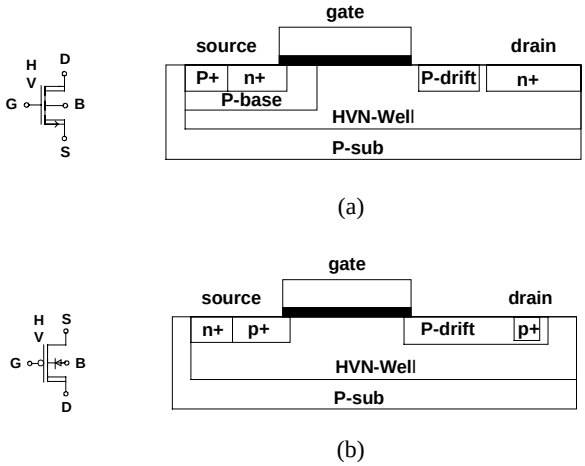

Fig. 3 Cross-sections of HV devices and corresponding symbols: (a) HV NMOS, (b) HV PMOS

B. Operation of voltage doubler circuit

To create a boosting DC voltage using the standard technologies, the n and p type transistors in the conventional voltage doubler circuit, are used like a switch where its breakdown voltages drain-source and bulk are limited by the technologies. To create a boosting high DC voltage, the conventional exponentially voltage doubler circuit [9] should be modified to meet the DALSA technology criteria of high voltage operation. Given that a HV transistor is unidirectional and cannot be used like a switch, a solution is adopted which is based on the use of the internal junction of the HV transistor. In fact, when a high voltage is applied on the floating source of the HVNMOS (figure 3a) with a low voltage on its drain, the diode formed by the P-base/HVN-Well junction conducts and transfers the HV signal to the drain. Similar for a HVPMOS transistor (figure 3b), when a HV is applied on its drain and a low voltage on its source, the diode formed by P-drift/HVN-Well junction conducts and tranfers the HV to its source. By using the HV transistors as switches in the voltage doubler circuit, the pumping capacitors cannot maintain a voltage higher than the input stage voltage due to the previous explanation. Doing so, the HV N and P type transistors are connected like it is shown in figure 2 and act as diodes with its dynamic resistor (R_D), and inherent constant diode voltage Vγ are controlled by gate-source voltage (V_{GS}). By increasing V_{GS}, the carrier profil will change and the R_D and Vγ will decrease.

The adapted votage doubler includes a level up shifter used in each stage of the VHVUC as a clock booster in order to increase the voltage exponentially by every stage which becomes power supplies for following cascaded stages. Its output are two phase non-overlapping clocks (CK_1 and CK_2) of which amplitudes are enlarged to (0, V_{low}). During the first half cycle, $CK_1 = V_{low}$, $CK_2 = 0$, the internal diodes of M_1 and M_4 condut; C_2 is charged to V_{low} through the M_1 diode, while C_1 is discharged to V_{high} (2 V_{low}), through M_4. During the second half cycle, $CK_1 = 0$, $CK_2 = V_{low}$, the internal diodes of M_2 and M_3 condut; C_1 is charged to V_{low} through the M_2 diode, while C_2 is discharged to V_{high} (2 V_{low}), through M_3. A voltage gain is therefore obtained between V_{low} and V_{high} and can be approximated by the following expression :

$$\Delta V = V_{low}\frac{C}{C + C_{par}} - 2\left[V_{\gamma} + \frac{I_{out}}{(C + C_{par})f}\right] \qquad (2)$$

where $C = C_1 = C_2$, C_{par} is the parasitic capacitance on the internal nodes of the stage and f is the operating frequency of the system. The output series resistance of each stage is given by

$$R_s = \frac{2}{(C + C_{par})f} \qquad (3)$$

In order to avoid the exceeding of the oxide BV of the charge transfer transistors M_3-M_4, during the increasing of the DC voltage from stage to another, a new technique is proposed (figure2). It is based on a level up stage, used to maintain on the gate of HVPMOS transistors, the same output stage DC voltage. To protect the gate oxide of the cross-connected HVNMOS transistors M_1-M_2, shown in figure 2, a technique is used, based on the divided DC voltage.

III. DESIGN OF THE DRIVE AMPLIFIER

In order to excite the ultrasonic transducer element for creating the ultrasound waves radiating into the load, a fully integrated drive amplifier is proposed (figure 4). It is based on a voltage level-up stage and a class D switching output stage. The power supply of the drive amplifier is connected to the output node of the described VHVUC. To create the shock excitation high-voltage pulse, the drive amplifier is triggerred by a three pulse signals Vp1,Vp2 and Vn1. The pulse duration is equal to $Q/2f$ [3], where Q is the dumping factor (range from 2 to 5) and f is the resonating frequency of transducer element which is 3.5 MHz for abdominal region. In such applications, the transducer element is poorly damped because of the impedance mismatch between it and the tissue and for a good compromise between the axial and lateral resolutions. The shape of electric excitation pulse generated by this drive amplifier is non-rectangular with an exponential slope. This signal shape is recommended in medical ultrasonic applications because it produces a shorter received echo signal without oscillation [10].

In order to avoid the output voltage drop of the VHVUC, M1 and M2 are turned off all the time of the pulse repetition. The electrical equivalent model of ultrasonic transducer element is shown in figure 4. The well-known model for a crystal, which is a series circuit of an inductance (L), a capacitor (C) and a resistor (R) and all are paralleled by a another capacitor (C_p). The inductance is used to increase the sensitivity of the transducer. The impedance of the transducer Z is given by the equation (4)

$$Z = \frac{\left(\omega^2 CL - 1\right) - j(\omega CR)}{\left(\omega^2 CC_p R\right) + j\left\{\omega^3 CC_p L - \omega\left(C + C_p\right)\right\}} \qquad (4)$$

where ω is the angler frequency. At the series resonant frequency the impedances of C and L cancel each other and Z becomes R//C_p. The presented ultrasonic transducer has a capacitive property because its input frequency (1/pulse width) is lower than the 3.5MHz resonating frequency. The RLC looks capacitive and can form a parallel resonance with C_p.

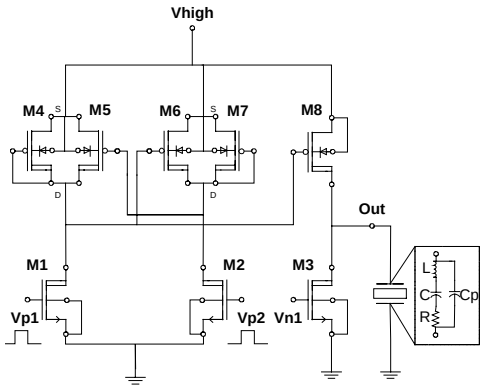

Fig. 4 Schematic of the drive amplifier for unidirectional excitation pulses.

IV. SIMULATION RESULTS

Table 1 shows the most significant characteristics of the VHVUC implemented using 0.8µm CMOS/DMOS High-Voltage process technology. The simulation was done with Spectre under CADENCE platform. For the VHVUC and the drive amplifier building blocks, the power consumption is around 360 mW (out of shock excitation) which is very low for any ultrasonic applications. The voltage gain factor, the output voltage ripples for 2 MHz frequencies, and the rise time show that the VHVUC has a good performance and is very adequate to a pulse wave ultrasonic system.

Figure 5 shows the results of the VHVUC step-up response using an input voltage of 10 V and a large output load capacitance of 100-pF to reduce the output voltage ripples. The output voltage reaches the steady state with a rise time of 150µs which is shorter than 260µs pulse repetition time. So, it is suitable for our application.

The simulation results of the drive amplifier supplied by the VHVUC during several triggering are shown in figure 6. A chain of current ulses coming from the transducer and voltage excitation pulses applied across the transducer are shown in figures 6(a) and 6(b) respectively. The pulse repetition time is fixed on 260µs which is equal to the time back and forth of the ultrasound wave for a maximum depth of 20cm into the human body and ultrasonic wave velocity of 1540 m/s. From figure 6(c), we can notice that the output voltage of the VHVUC reachs the required steady state with a rise time of 150µs.

Figure 7 shows the response of the drive amplifier for a single shock excitation pulse of 140 V spike at the transducer element with a current waveform range between 25 mA and –24 mA going towards the transducer element. The peak dissipated power in the transducer element is 3.5 Watts. A relatively short received signal with high amplitude is obtained when using high excitation voltage. The current pulse has a rise time of 220 ns and a fall time of 713 ns with a dumping factor of 4. The cause of the increasing of the rise time is due to the on resistance of the switch M8.

Table 1. Spectre simulation of the proposed VHVUC

Characteristics	Value
Voltage gain factor	83 %
No. of stages	5
Input voltage	10 Volts
Output voltage	200 Volts
Oscillator frequency	2 MHz
Power consumption	360 mW
Output voltage ripples	95 mVolts
Output current	512 µA
Power supply	5 Volts
Rise time	150µs
Technology	CMOS/DMOS 0.8µm

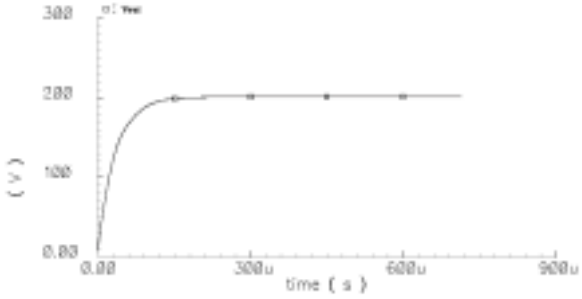

Fig. 5 Simulation of step-up response for VHVUC with 100-pF capacitive load

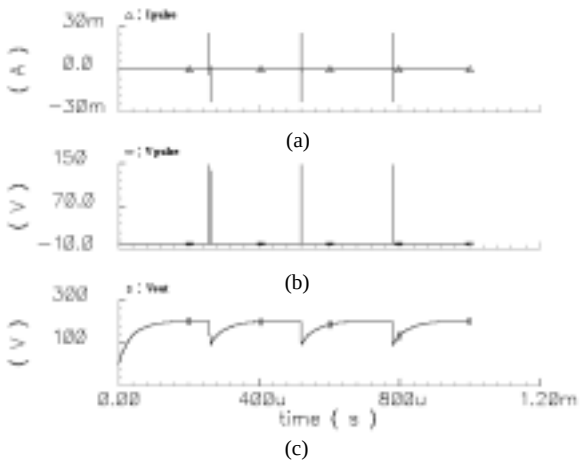

Fig. 6 (a) Chain of the current waveforms, (b) Chain of the voltage waveforms across the transducer, (c) Output voltage of the VHVUC

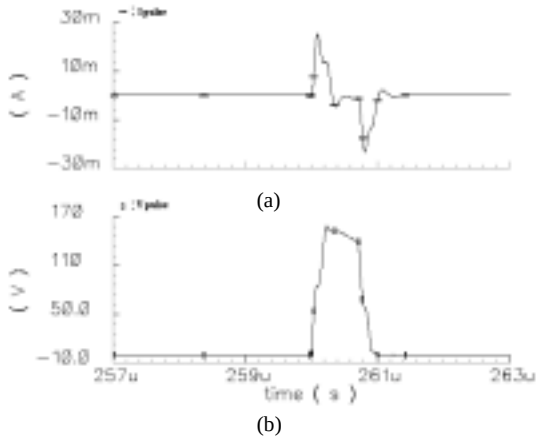

Fig. 7 (a) Current waveform with a peak of 25 mA, (b) single Shock excitation pulse with an amplitude of 140V

V. CONCLUSION

The realization of a new fully integrated up converter followed by a drive amplifier which are dedicated to ultrasonic transmitter have been described. The proposed VHVUC is based on 5 stages of voltage doubler circuits adapted to the DALSA 0.8µm CMOS/DMOS High-Voltage process technology. A voltage level-up Shifter is used in each stage as a clock generator in order to increase the voltage exponentially with stages. The proposed drive amplifier is based on a level-up stage and a class D switching output satge. Several difficulties arising at high voltage circuit implementation are and design optimizations were presented. The simulation results of the VHVUC, comfirme its ability to deliver the 200 DC voltage needed in medical ultrasonic imaging and in other applications such like driving MEMS and plasma display. The drive amplifier offers good performances with high voltage shock excitation pulse suitable for diagnostic ultrasonic imaging. The fully integration of these blocks shows several advantages: low noise, low consumption, high precision, good bulk and high voltage adequate for the future portable ultrasonic devices.

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