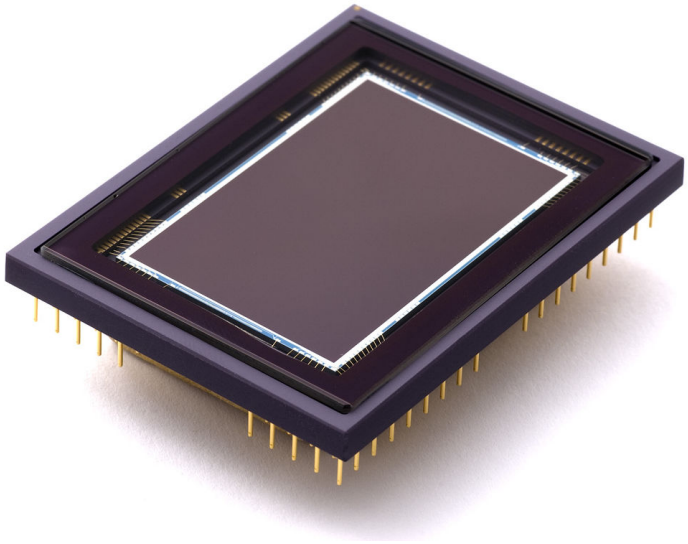
DATA SHEET



FTF6040M

24M Full-Frame CCD Image Sensor

Product Specification

March 2011

Teledyne DALSA
Professional Imaging

TELEDYNE DALSA
A Teledyne Technologies Company

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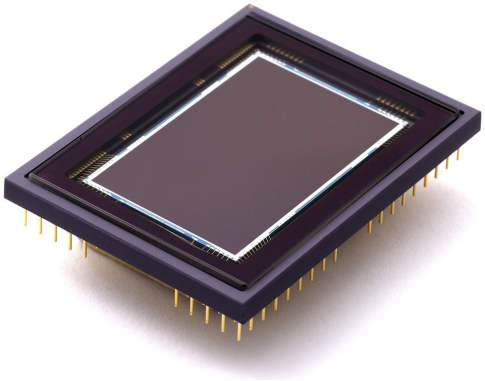
24M Full-Frame CCD Image Sensor FTF6040M

- **35mm film compatible image format (36 x 24mm^2)**
- **24M active pixels (6000H x 3988V)**
- **Progressive scan**
- **Excellent anti-blooming**
- **Variable electronic shuttering**
- **Square pixel structure (6.0μm x 6.0μm)**
- **H and V binning**
- **Vertical sub-sampling**
- **>70% fill factor**
- **Wide angular response**
- **High dynamic range (>71dB)**
- **High sensitivity**
- **Low dark current and low fixed pattern noise**
- **Low readout noise**
- **Data rate up to 25 MHz per output**
- **Mirrored and split readout**
- **Perfectly matched to visual spectrum**
- **RoHS compliant**



1. Description

The FTF6040M is a full-frame monochrome CCD image sensor designed for demanding applications like medical, scientific and industrial, with very low dark current and a linear dynamic range of over 11 true bits. High quantum efficiency is achieved by using transparent membrane poly-silicon electrodes. Metal strapping allows high-speed vertical and horizontal transport. The four low-noise output amplifiers, one at each corner of the chip, make the FTF6040M suitable for a wide range of high-end visual light applications. With one output amplifier, a progressively scanned image can be read out at 0.9 frames per second. By using two outputs, the frame rate increases accordingly. The device structure is shown in figure 1.

Device structure

Optical size:	36.000 mm (H) x 23.928 mm (V)			
Chip size:	37.824 mm (H) x 25.682 mm (V)			
Pixel size:	6.0 μm x 6.0μm			
Active pixels:	6000 (H) x 3988 (V)			
Total no. of pixels:	6048 (H) x 4074 (V)			
Optical black pixels:	Left:	20	Right:	20
Overscan pixels:	Left:	4	Right:	4
Optical black lines:	Bottom:	6	Top:	6
Dummy lines :	Bottom:	33	Top:	33
Overscan lines:	Bottom:	4	Top:	4
Dummy register cells:	Left:	23	Right:	23

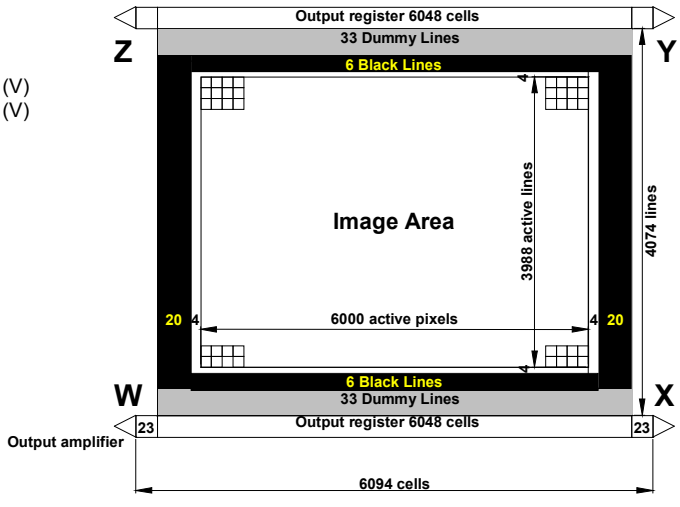


Figure 1 – Device Structure

2. Architecture of the FTF6040M

The optical centers of all pixels in the image section form a square grid. The charge is generated and integrated in this section. Output registers are located below and above the image section for readout. After the integration time, the image charge is shifted one line at a time to either the upper or lower register, depending on the selected readout mode. A separate transfer gate (TG) between the image section and output register allows vertical sub-sampling. The left and right half of each register can be controlled independently. This enables either single or multiple readout. During vertical transport, the C3 gates separate the pixels in the register. The central C3 gates of the lower and upper registers are part of the left half of the sensor (W and Z quadrants respectively). Each register can be used for vertical binning. Each register contains a summing gate at both ends that can be used for horizontal binning (see figure 2). The charge-to-voltage conversion is performed by a three-stage source follower amplifier (4 in total). The charge-to-voltage conversion node is reset to reset-drain voltage (RD) by pulsing the reset gate (RG). The amplifier power supply is SFD, the ground terminal is SFS. VNS and VPS are the bias voltages for the n-type substrate and for the CCD p-well, respectively.

IMAGE SECTION	
Image diagonal (active video only)	43.226 mm
Aspect ratio	3:2
Active image width x height	36.000 x 23.928 mm^2
Pixel width x height	6.0 x 6.0 μm^2
Fill factor	>70%
Image clock pins	16 (4 x 4) pins (A1...A4)
Capacity of each clock phase	200nF per phase
Total number of lines	4074
Number of active lines	3988
Number of edge lines	8 (=2x4)
Number of black lines	12 (=2 x 6)
Number of dummy lines	66 (=2 x 33)
Total number of pixels per line	6048
Number of active pixels per line	6000
Number of over scan (timing) pixels per line	8 (2 x 4)
Number of black reference pixels per line	40 (2 x 20)

OUTPUT REGISTERS	
Number of output registers	2 (1 top, 1 bottom)
Number of dummy cells per register	46 (2 x 23)
Number of register cells per register	6094 (6048 + 46)
Output register horizontal transport clock pins	3 pins per left/right register part (C1...C3)
Capacity of each C-clock phase	100 pF per pin
Overlap capacity between neighboring C-clocks	40 pF
Output register Summing Gates	4 pins, one per output (SG)
Capacity of each SG	15pF
Reset Gate clock phases	4 pins, one per output (RG)
Capacity of each RG	15pF
Output amplifier type	Three-stage source follower

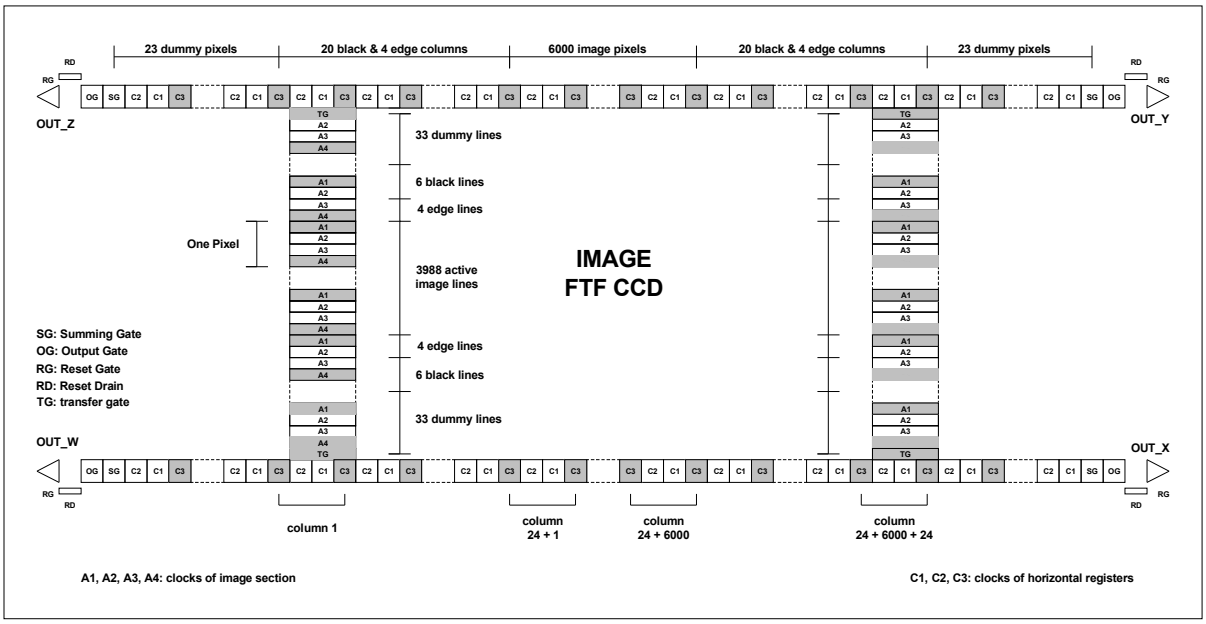


Figure 2: Detailed internal structure

3. Operating Conditions

3.1 Absolute Maximum Ratings

ABSOLUTE MAXIMUM RATINGS[1]	MIN	MAX	UNIT
GENERAL:			
Storage temperature	-40	+80	ºC
Ambient temperature during operation	-20	+60	ºC
Voltage between any two gates	-20	+20	V
DC current through any clock (absolute value)	-0.2	+0.2	µA
OUT current (no short circuit protection)	0	+10	mA
VOLTAGES IN RELATION TO VPS:			
VNS, SFD, RD	-0.5	+30	V
SFS	-8	+5	V
All other pins (except RG)	-20	+25	V
VOLTAGES IN RELATION TO VNS:			
SFD, RD	-15	+0.5	V
SFS, VPS	-30	+0.5	V
All other pins (except RG)	-30	+0.5	V
VOLTAGES IN RELATION TO SFD:			
RD	-5	0	V
RG Voltage	0	+30	V

[1] During Charge reset it is allowed to exceed maximum rating levels in relation to VNS, according to the specified DC voltage settings (3.3) and AC clock level conditions (3.4).

3.2 Note on Voltage Settings

Since the AC signals for operating the horizontal register (register clocks C1-C2- C3, summing gate SG) and the output stage (reset gate RG) are analog signals for the CCD, the optimal voltage settings can be influenced by the waveforms of these signals, which in turn depend on the layout and schematics of the camera electronics. Thus the optimal value of all DC biases mentioned can deviate up to +/- 1V from the 'typical' values mentioned in the data sheets depending on the precise implementation of the hardware around the sensor.

3.3 DC Voltage Settings

DC CONDITIONS[1, 2]		MIN [V]	TYPICAL [V]	MAX [V]	MAX [mA]
VNS[3]	n-substrate	20	adjusted	28	15
VPS	p-well	5.5	6	6.5	15
SFD	Source Follower Drain	19.5	20	20.5	4.5
SFS	Source Follower Source	0	0	0	1
VCS	Current Source	0	0	0	–
OG	Output Gate	5.75	6.0	6.25	–
RD	Reset Drain	19.5	20	20.5	–

[1] All voltages in relation to SFS; typical values are according to test conditions.
[2] Power-up sequence: VNS, SFD, RD, VPS, all others. The difference between SFD and RD should not exceed 5V during power up or down.
[3] To set the VNS voltage for optimal Vertical Anti-blooming (VAB), it should be adjustable between minimum and maximum values.

3.4 AC Clock Level Conditions

The following voltages should be applied for operating the sensor.
A clocking scheme of 2 gates integrating and 2 gates blocking should be used.

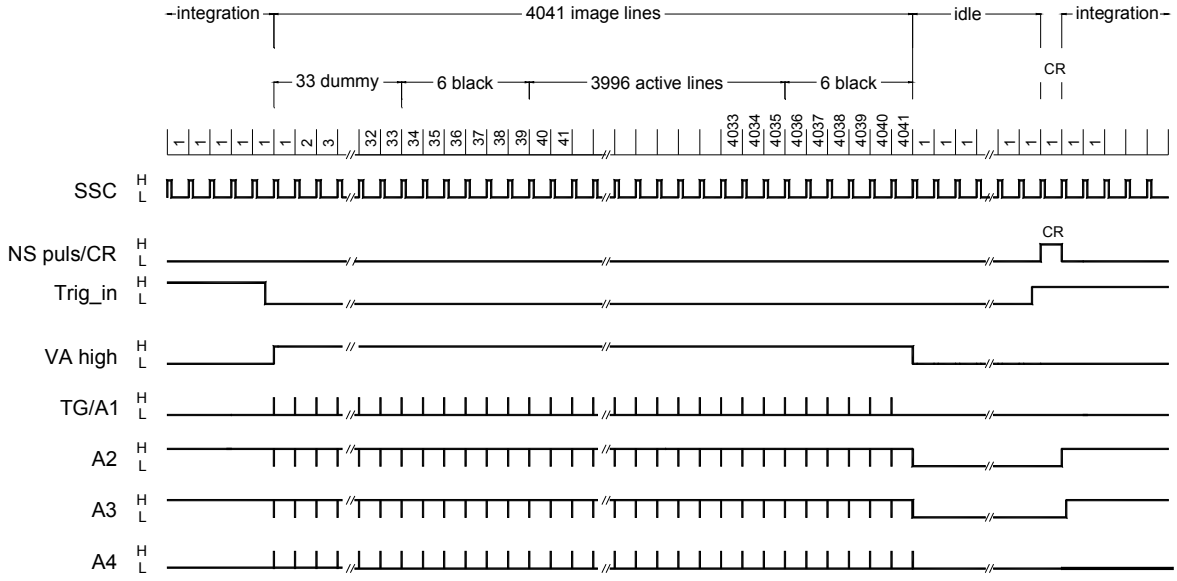
AC CLOCK LEVEL CONDITIONS[1]	MIN	TYPICAL	MAX	UNIT
IMAGE CLOCKS/ TRANSFER GATES[2]				
A-clock amplitude during integration and hold		10		V
A-clock amplitude during vertical transport (duty cycle=5/8)[3]		10.8		V
A-clock low level	-	0	-	V
Charge reset (CR) level on A-clock[4]	0	0	0	V
OUTPUT REGISTER CLOCKS:				
C-clock amplitude (duty cycle during hor. transport=3/6)	4.75	5	5.25	V
C-clock low level	-	3.5	-	V
Summing Gate (SG) amplitude	4.75	5.0	10	V
Summing Gate (SG) low level	-	5	-	V
OTHER CLOCKS:				
Reset Gate (RG) amplitude	5	5	10	V
Reset Gate (RG) low level	-	17.5	-	V
Charge Reset (CR) pulse on VNS[4]	0	5	5	V

[1] All voltages in relation to SFS; typical values are according to test conditions.
[2] Transfer gate should be clocked as A1 during normal transport or held low during a line shift to sub-sample image.
[3] Three-level clock is preferred for maximum charge;
A two level clock can be used if a lower maximum charge handling capacity is allowed
[4] Charge Reset is achieved by applying the typical A-clock low level to all image clocks and simultaneously applying the Charge Reset pulse on VNS

3.5 Timing diagrams (for default operation)

AC CHARACTERISTICS	MIN	TYPICAL	MAX	UNIT
Horizontal frequency (1/Tp)[1]	-	25		MHz
Vertical frequency	-	50		kHz
Charge Reset (CR) time	10	Line time	-	µs
Rise and fall times: image clocks (A)	10	20	-	ns
register clocks (C)[2]	3	5	1/8 Tp	ns
summing gate (SG)	3	5	1/8 Tp	ns
reset gate (RG)	-	3	1/8 Tp	ns

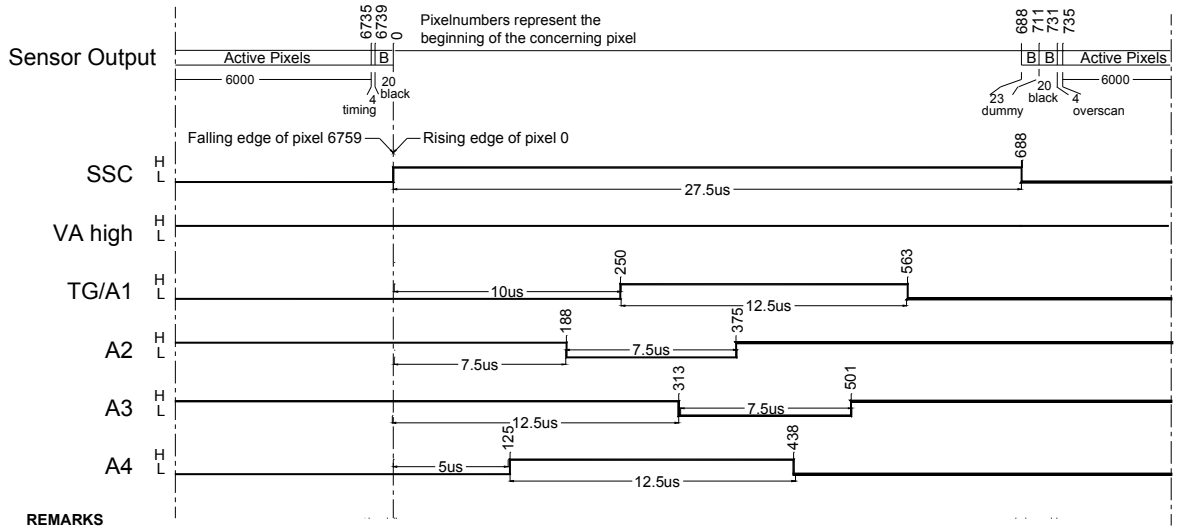
[1] TP = 1 clock period
[2] Duty cycle = 3/6



REMARKS
* CR is applied during the first line after the transition from L to H of Trig_in
* CCD is integrating during high period of Trig_in
* After readout sequence the timing will go into idle mode.

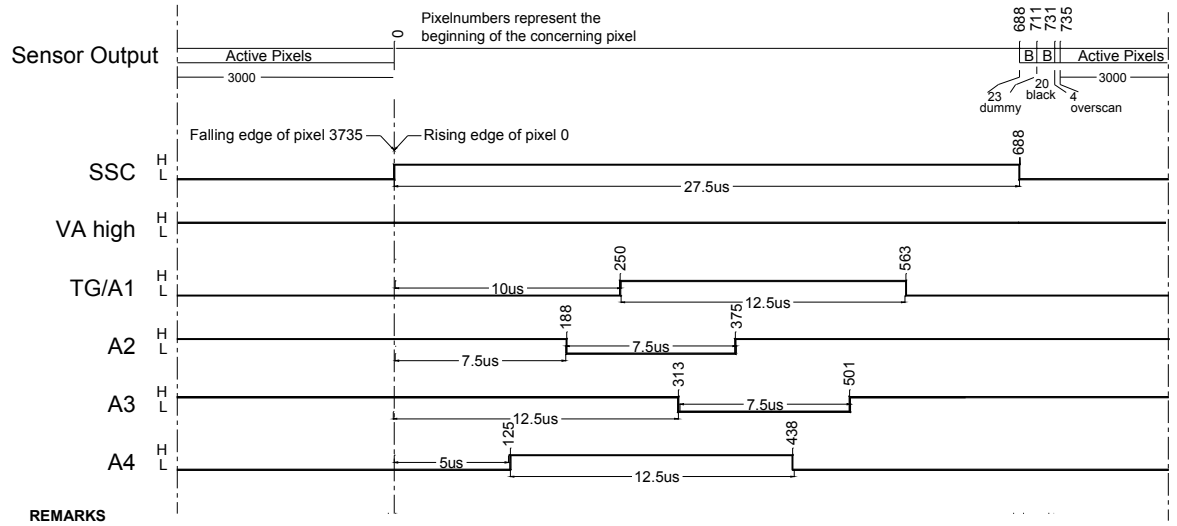
Figure 3: Frame Timing Diagram

Line Timing, Single Output Mode



REMARKS
* Single output
* Thorizontal = 6759 * 1/25E6 = 270.36us
* Vertical transport frequency = 50kHz

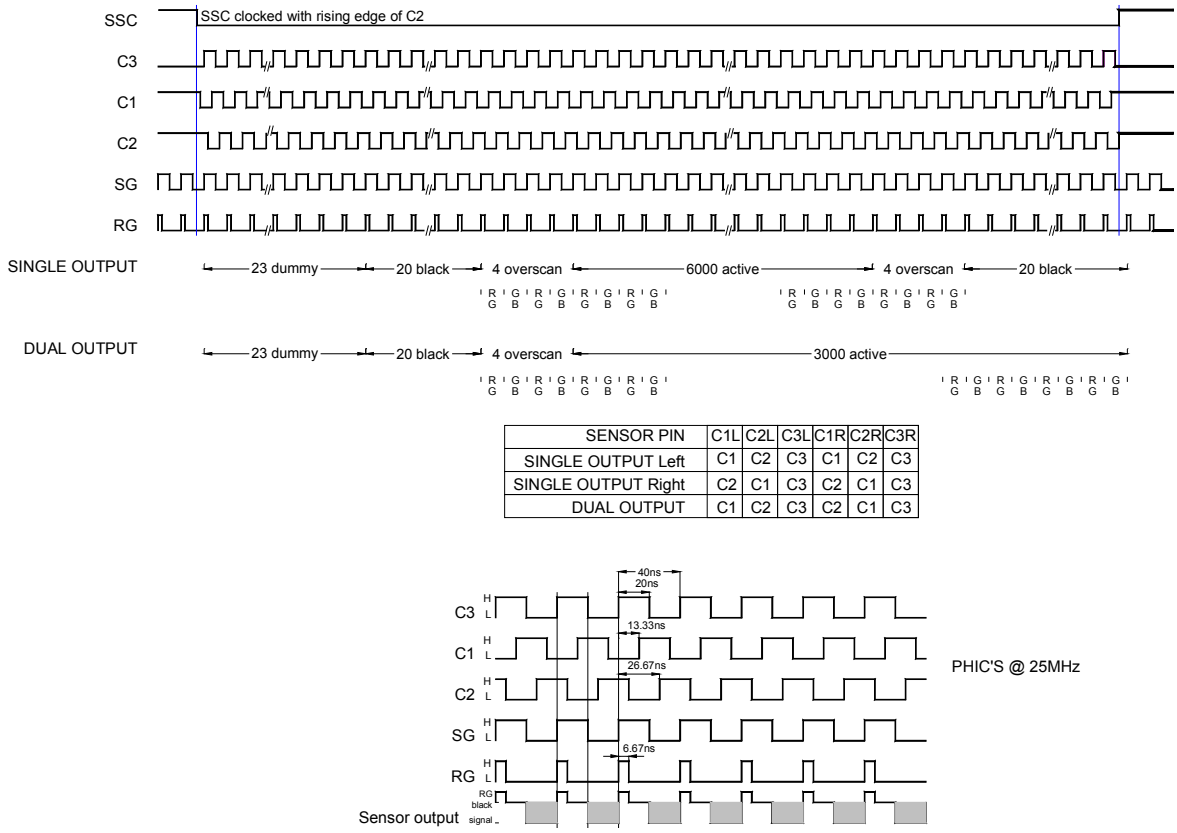
Line Timing, Dual Output Mode



REMARKS
* Dual output
* Thorizontal = 3735 * 1/25E6 = 149.4us
* Vertical transport frequency = 50kHz

Figure 4: Vertical Readout, Single and Dual Output Modes

Pixel Timing



SENSOR PIN	C1L	C2L	C3L	C1R	C2R	C3R
SINGLE OUTPUT Left	C1	C2	C3	C1	C2	C3
SINGLE OUTPUT Right	C2	C1	C3	C2	C1	C3
DUAL OUTPUT	C1	C2	C3	C2	C1	C3

Figure 5: Horizontal Readout, Single and Dual Output Modes

4. Performance

The test conditions for the performance characteristics are as follows:

- All values are measured using typical operating conditions.
- VNS is adjusted as low as possible while maintaining proper vertical anti-blooming
- Sensor temperature = 60°C (333K)
- Horizontal transport frequency = 25MHz
- Vertical transport frequency = 50kHz
- Integration time = 100ms

LINEAR OPERATION	MIN	TYPICAL	MAX	UNIT
Charge Transfer Efficiency[1]	-	0.999999	-	-
Image lag	-	0	0	%
Resolution (MTF) @ 83.3 lp/mm	65	-	-	%
Peak Quantum Efficiency (530nm)	-	37	-	%
Sensitivity @3200K without IR cut off filter [2]		135		kel/lux.s
Sensitivity @3200K with IR cut off filter [2]		55		kel/lux.s
Stitching effect		1	3	%
Low Pass Shading[3]		2	5	%
Random Non-Uniformity (RNU)[4]		1	2	%

[1] Charge Transfer Efficiency values are tested by evaluation and expressed as the value per gate transfer
[2] Sensitivity @3200K is measured using a halogen light source, without or with a 1.7mm thick BG40 infrared cut-off filter placed in front of the sensor.
[3] Low Pass Shading is defined as the ratio of the one-σ value of an 8x8 pixel blurred image (low-pass) to the mean signal value
[4] RNU is defined as the ratio of the one-σ value of the high-pass image to the mean signal of nominal light

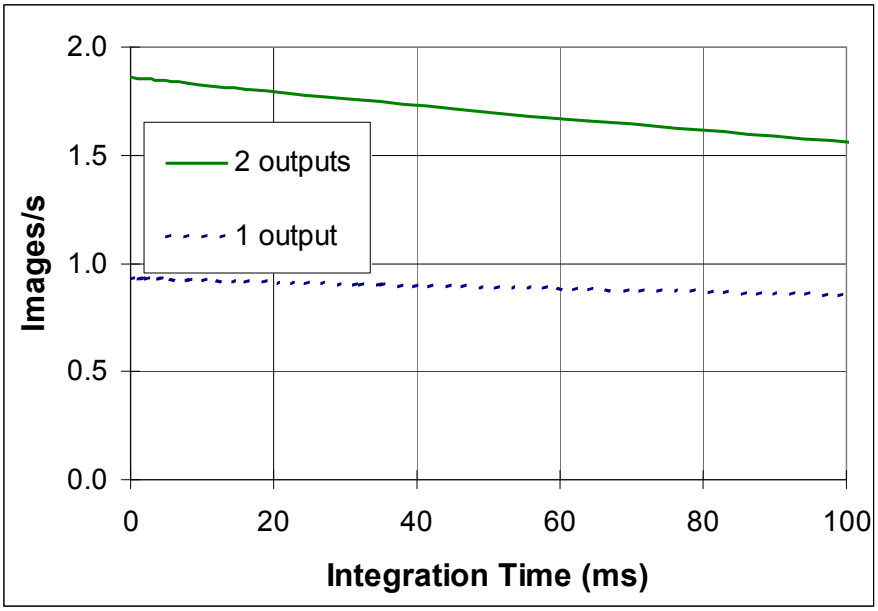


Figure 6: Maximum number of images/second versus integration time

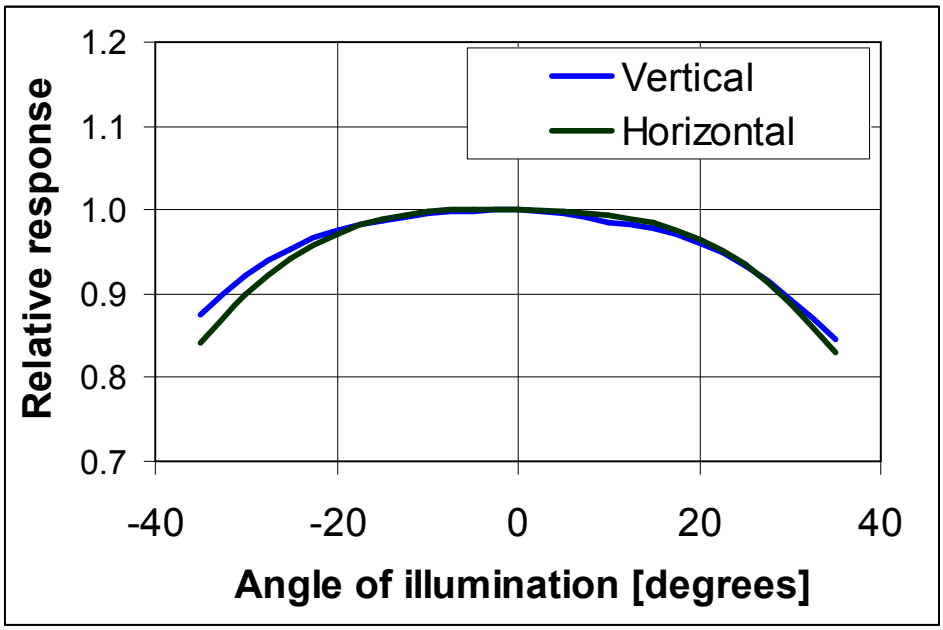


Figure 7: Angular response versus angle of illumination

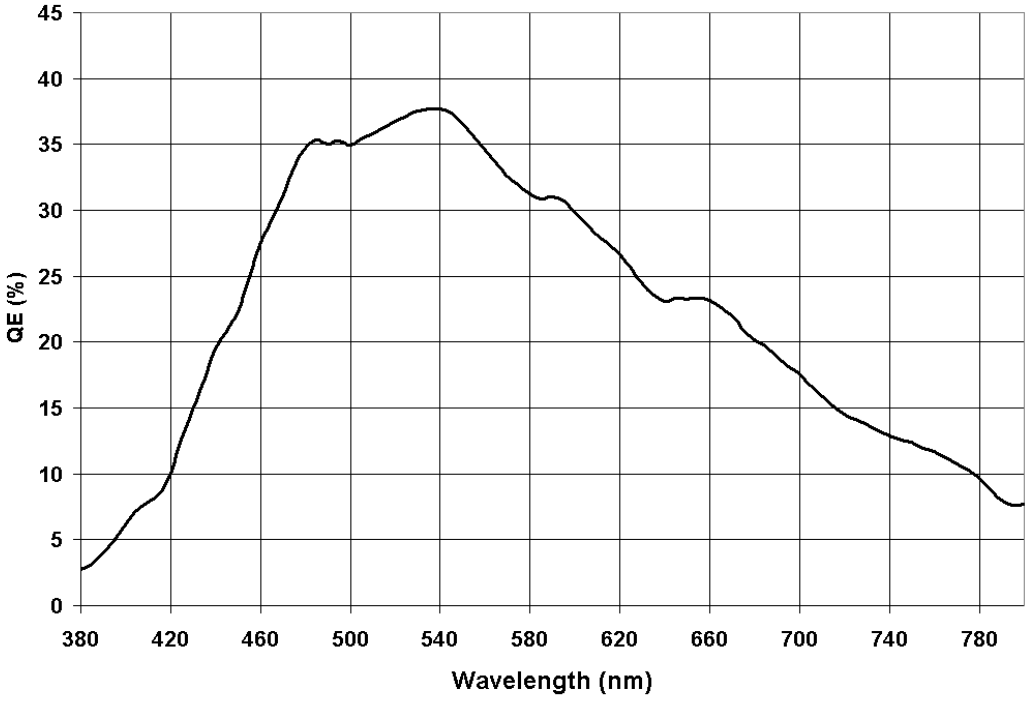


Figure 8: Quantum Efficiency versus wavelength

LINEAR/SATURATION	MIN	TYPICAL	MAX	UNIT
Full-well capacity saturation level (Qmax)[1]	-	43000	-	el
Full-well capacity linear operation (Qlin)[2]	-	38000	-	el
Overexposure[3] handling	-	200	-	x Qmax level
Dynamic range		71.8		dB
Linear dynamic range		70.7		dB

[1] Qmax is determined from the low-pass filtered image
[2] The linear full-well capacity Qlin is calculated from linearity test (see dynamic range). The test guarantees 97% linearity.
[3] Overexposure over entire area while maintaining good Vertical Anti-Blooming (VAB) is tested by measuring the dark lines along the image section.

OUTPUT BUFFERS	MIN	TYPICAL	MAX	UNIT
Conversion factor	35	37	39	µV/el.
Mutual conversion factor mismatch (ΔACF)[1]	-	0	3	µV/el.
Supply current	-	4.5	-	mA
Bandwidth (R_{load}=3.3 KΩ)	110	130	-	MHz
Output impedance buffer (R_{load}=3.3 KΩ, C_{load}=2pF)	-	250	-	Ω
Amplifier noise over full bandwidth after CDS	-	11	-	el

[1] Mismatch of the four outputs is specified as ΔACF with respect to reference measured at the operating point (Q_{lin}/2)

DARK CONDITION	MIN	TYPICAL	MAX	UNIT
Dark current level @ 20°C	-	4	6	pA/cm^2
Dark current level @ 60°C	-	120	200	pA/cm^2
Fixed Pattern Noise[1] (FPN) @ 60ºC	-	500		el/s

[1] FPN is one-σ value of the high-pass image and normalized at 1 sec integration time

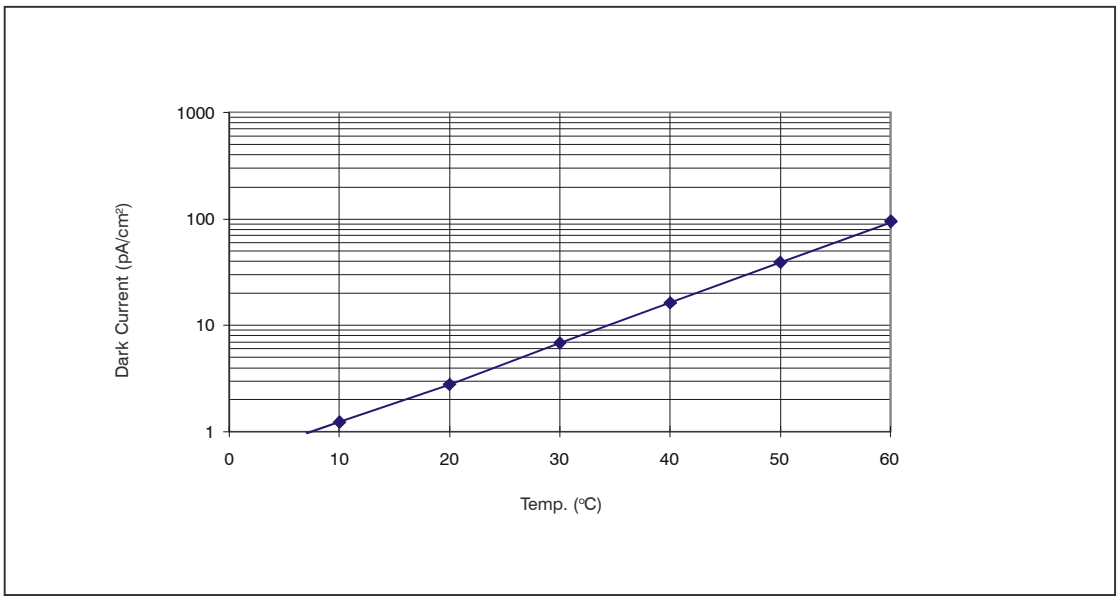


Figure 9: Dark current versus temperature

5. Application information

Current handling
One of the purposes of VPS is to drain the holes that are generated during exposure of the sensor to light. Free electrons are either transported to the VRD connection and, if excessive (from overexposure), free electrons are drained to VNS. No current should flow into any VPS connection of the sensor. During high overexposure, a total current of 5 to 10mA through all VPS connections together may be expected. The pnp emitter follower in the circuit diagram (figure 12) serves these current requirements.

VNS drains superfluous electrons as a result of overexposure. In other words, it only sinks current. During high overexposure, a total current of 5 to 10mA through all VNS connections together may be expected. The clamp circuit, consisting of the diode and electrolytic capacitor, enable the addition of a Charge Reset (CR) pulse on top of an otherwise stable VNS voltage. To protect the CCD, the current resulting from this pulse should be limited. This can be accomplished by designing a pulse generator with a rather high output impedance.

Decoupling of DC voltages
All DC voltages (not VNS, which has additional CR pulses as described above) should be uncoupled with a 22nF uncoupling capacitor. This capacitor must be mounted as close as possible to the sensor pin. Further noise reduction (by bandwidth limiting) is achieved by the resistors in the connections between the sensor and its voltage supplies. The electrons that build up the charge packets that will reach the floating diffusions only add up to a small current, which will float through VRD. Therefore, a large series resistor in the VRD connection may be used.

Outputs
To limit the on-chip power dissipation, the output buffers are designed with open source outputs. Outputs to be used should therefore be loaded with a current source or more simply with a resistance to GND. In order to prevent the output (which typically has an output impedance of about 250Ω) from bandwidth limitation as a result of capacitive loading, load the output with an emitter follower built from a high-frequency transistor. Mount the base of this transistor as close as possible to the sensor and keep the connection between the emitter and the next stage short. The CCD output buffer can easily be destroyed by ESD. By using this emitter follower, this danger is suppressed; do NOT reintroduce this danger by measuring directly on the output pin of the sensor with an oscilloscope probe. Instead, measure on the output of the emitter follower. Slew rate limitation is avoided by avoiding a too-small quiescent current in the emitter follower; about 10mA should do the job. The collector of the emitter follower should be uncoupled properly to suppress the Miller effect from the base-collector capacitance.

A CCD output load resistor of 3.3kΩ typically results in a bandwidth of 130 MHz for the outputa.

Device protection
The output buffers of the FTF6040M are likely to be damaged if VPS rises above SFD or RD at any time. This danger is most realistic during power-on or power-off of the camera. The RD voltage should always be lower than the SFD voltage.

Never exceed the maximum output current. This may damage the device permanently. The maximum output current should be limited to 10mA. Be especially aware that the output buffers of these image sensors are very sensitive to ESD damage.

Because of the fact that our CCDs are built on an n-type substrate, we are dealing with some parasitic npn transistors. To avoid activation of these transistors during switch-on and switch-off of the camera, we recommend the application diagram of figure 12.

Unused sections
To reduce power consumption, the following steps can be taken. Connect unused output register pins (C1...C3, SG, OG) and unused SFS pins to zero Volts.

6. Device Handling

An image sensor is an MOS device, which can be destroyed by electro-static discharge (ESD). Therefore, the device should be handled with care.

Always store the device with short-circuiting clamps or on conductive foam. Always switch off all electric signals when inserting or removing the sensor into or from a camera (the ESD protection in the CCD image sensor process is less effective than the ESD protection of standard CMOS circuits).

Being a high quality optical device, it is important that the cover glass remains undamaged. When handling the sensor, use finger cots.

When cleaning the glass, we strongly recommend using ethanol. Use of other liquids is strongly discouraged:

- if the cleaning liquid evaporates too quickly, rubbing is likely to cause ESD damage.
- the cover glass and its coating can be damaged by other liquids.

Rub the window carefully and slowly.

Dry rubbing of the window may cause electro-static charges or scratches, which can destroy the device.

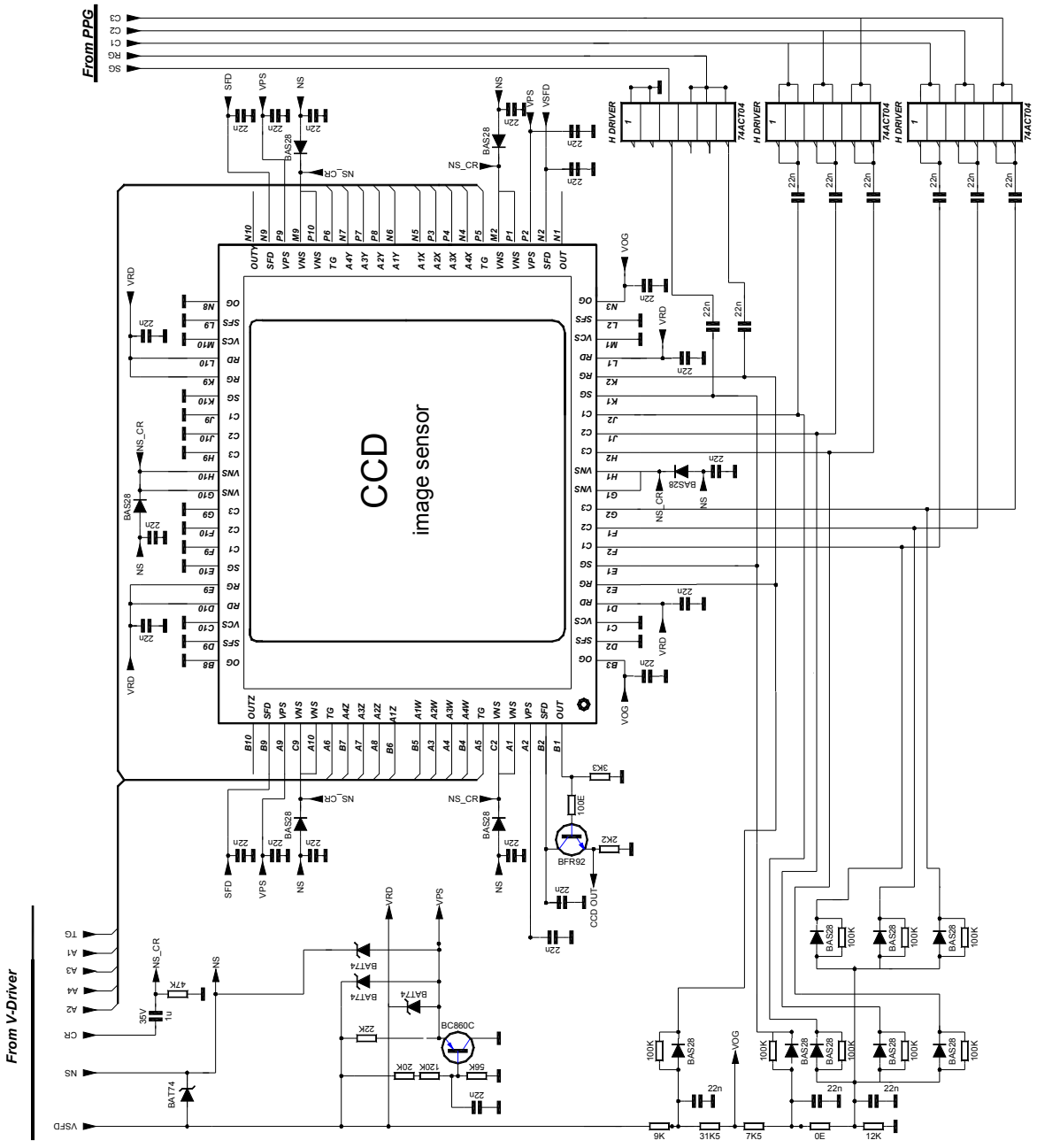


Figure 10: Application diagram for single output operation

7. Pin configuration

The FTF6040M is mounted in a Pin Grid Array (PGA) package with 96 pins in a 20x15 grid of 48.26 x 35.56mm^2. The position of pin A1 (quadrant W) is marked with a gold dot on top of the package. The image clock phases of quadrant W are internally connected to X, and those of Y are connected to Z.

SYMBOL	FUNCTION	PIN # W	PIN # X	PIN # Y	PIN # Z
VNS	n-substrate	A1	P1	P10	A10
TG	Transfer Gate	A5	P5	P6	A6
VNS	n-substrate	C2	M2	M9	C9
VNS	n-substrate	G1	H1	H10	G10
VPS	p-well	A2	P2	P9	A9
SFD	Source Follower Drain	B2	N2	N9	B9
SFS	Source Follower Source	D2	L2	L9	D9
VCS	Current Source	C1	M1	M10	C10
OG	Output Gate	B3	N3	N8	B8
RD	Reset Drain	D1	L1	L10	D10
A1	Image Clock (Phase 1)	B5	N5	N6	B6
A2	Image Clock (Phase 2)	A3	P3	P8	A8
A3	Image Clock (Phase 3)	A4	P4	P7	A7
A4	Image Clock (Phase 4)	B4	N4	N7	B7
C1	Register Clock (Phase 1)	F2	J2	J9	F9
C2	Register Clock (Phase 2)	F1	J1	J10	F10
C3	Register Clock (Phase 3)	G2	H2	H9	G9
SG	Summing Gate	E1	K1	K10	E10
RG	Reset Gate	E2	K2	K9	E9
OUT	Output	B1	N1	N10	B10

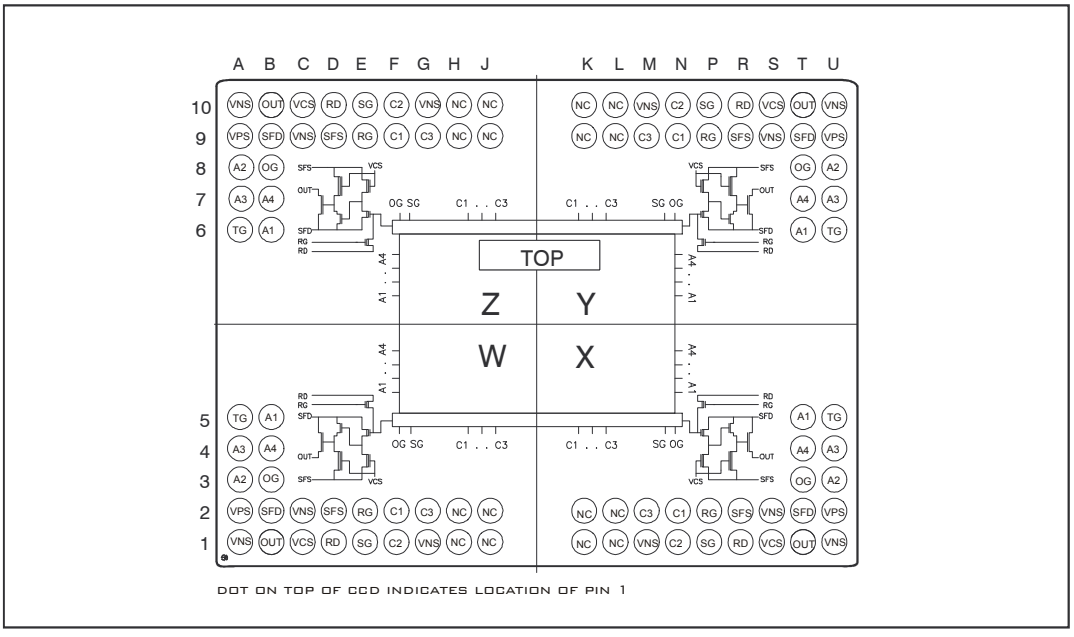


Figure 11: Pin configuration (top view)

8. Package information

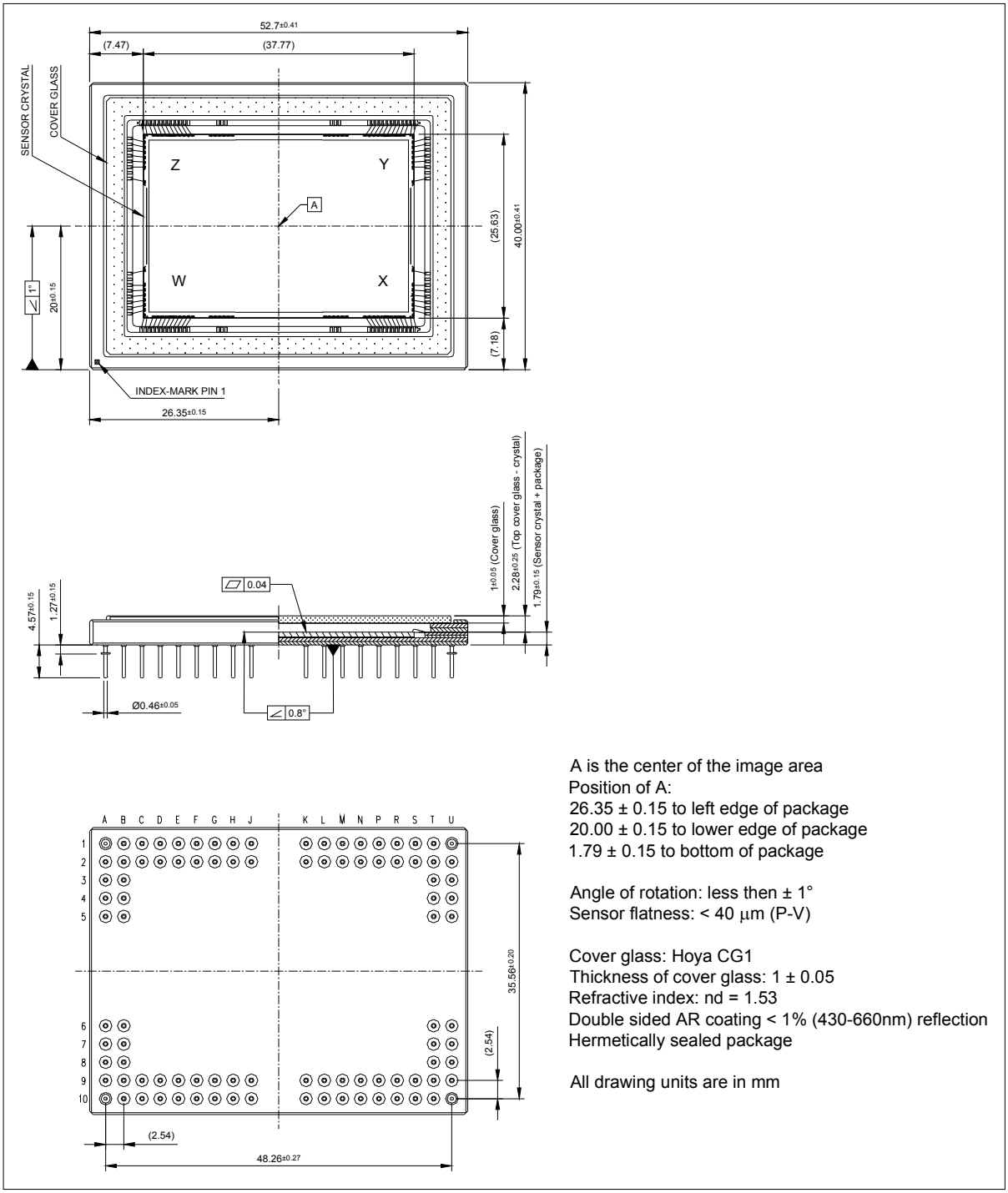


Figure 12: Mechanical drawing of the PGA package

9. Order codes

The sensor can be ordered using the following code:

FTF6040M sensor		
Description	**Quality Grade**	**Order Code**
FTF6040M/HG	High Grade	9922 157 86311
FTF6040M/IG	Industrial Grade	9922 157 86321
FTF6040M/EG	Economy Grade	9922 157 86351
FTF6040M/TG	Test Grade	9922 157 86331

Defect Specifications

The CCD image sensor can be ordered in a specific quality grade. The grading is defined with the maximum amount of pixel defects, column defects, row defects and cluster defects, in both illuminated and non-illuminated conditions. For detailed grading information, please contact your local Teledyne DALSA representative.

For More Information

For more detailed information on this and other products, contact your local rep or visit our Web site at http://www.teledynedalsa.com/sensors/products/products.asp.

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