SAADC 37.5MS/s12bGF40lp

Successive approximation ADC

Features

- sample-rate up to 37.5 MS/s
- scalable full-scale input range 0.4-0.6 $V_{PP,SE}$
- low power consumption 6.3 mW
- differential mode
- 62 dB SNR
- 70 dB SFDR (incl THD)
- 12 bits, 10 ENOB
- 0.03 mm^2 in baseline 40 nm CMOS

Applications

- Multi-mode digital receivers
- Cable modems
- Video digitizing and CCD imaging
- Portable instrumentation
- Medical imaging

General description

This datasheet describes a general purpose Analog to Digital Converter (ADC) for low-power applications. The converter is a charge-redistribution successive-approximation type converter, and it is suitable to operate in a time-interleaved ADC to enable higher sample-rates. As an example, this ADC is applied in a 2.5 GS/s ADC system.

The key feature of this ADC is its low power consumption. Next to this, the full-scale range is programmable and its area is small.

The functional block diagram is shown in Figure 1.

The IP product described in this datasheet is silicon proven. The 2.5 GS/s ADC system in which this ADC is applied fulfills all mass-production consumer electronics requirements.

Block diagram

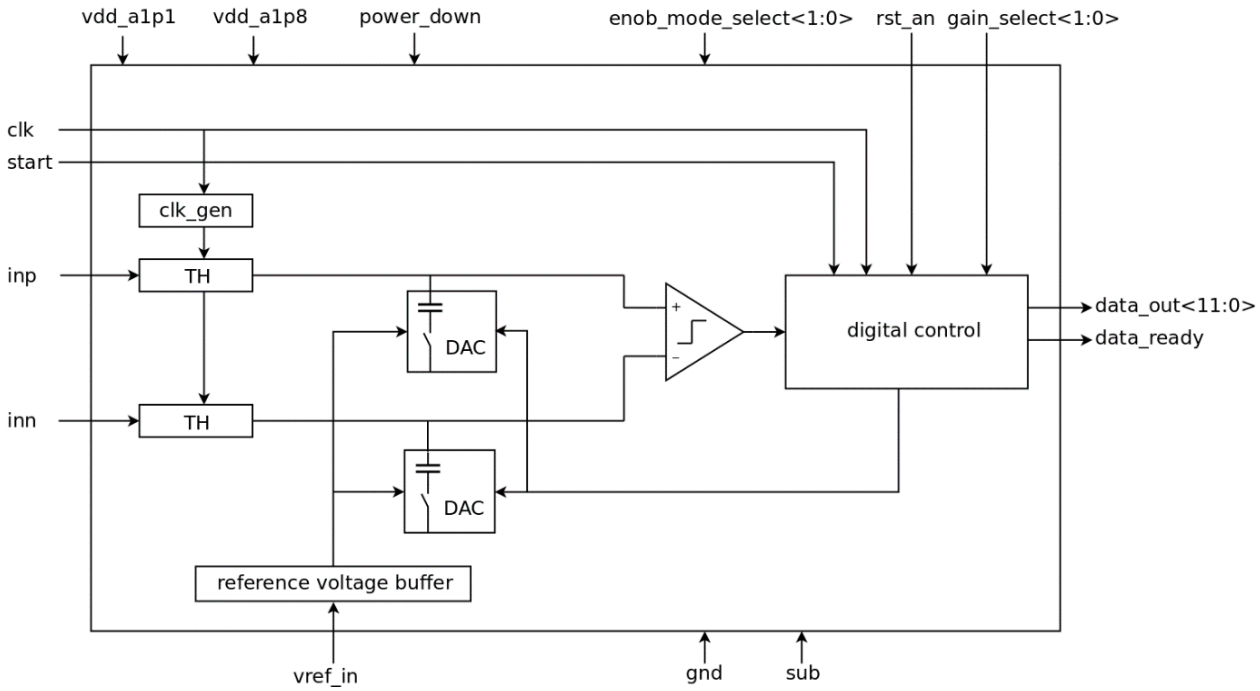

Figure 1: Block diagram of the Successive Approximation ADC

Specifications

Electrical Specifications

Parameter	Description	Min	Typ	Max	Units
f_S	Sample-rate		37.5		MS/s
f_{CLK}	Clock frequency		18		f_S
V_{DD1p1}	Supply voltage	1.1	1.15	1.2	V
V_{DD1p8}	Supply voltage	1.7	1.8	1.9	V
V_{FS}	Full-scale input voltage (programmable)	0.4	0.5	0.6	$V_{PP,SE}$
C_{IN}	Input capacitance (single-ended)		1.5		pF
P_{ADC}	Power consumption ADC		6.3		mW
$P_{BANDGAP}$	Power optional bandgap reference[1]		3.0		mW
Performance					
SFDR	Spurious Free Dynamic Range (including harmonics)		70[2]		dB
SNR	Signal to Noise Ratio		63		dB
DR	Dynamic Range		67		dB
ENOB	Effective Number Of Bits		10		bits
DNL	Differential Non-Linearity		1.5[2]		LSB
INL	Integral Non-Linearity		2[2]		LSB
Implementation					
Area	Die area in 40 nm CMOS		0.03		mm^2

Table 1: Specifications of the Analog-to-Digital Converter
Note[1]:A bandgap reference is available as a separate IP block, see section Options.
Note[2]: Estimation, since the linearity is limited by an input buffer. Measurements are being prepared to determine the actual ADC linearity.

Port list

Port name	Width	Description
GND	1	Ground
SUB	1	Substrate connection
VDD_A1P1	1	Analog 1.1V supply voltage
VDD_A1P8	1	Analog 1.8V supply voltage
VREF_IN	3	Reference voltage, only capacitively loaded
INP	1	Non-inverting analog input signal
INN	1	Inverting analog input signal
CLK	1	Clock signal at $18 \cdot f_S$
START	1	Signal that triggers the start of a new conversion
RST_AN	1	Asynchronous, active low, reset signal that sets the ADC in a well-defined state
POWER_DOWN	1	Power down signal, disables all static current
ENOB_MODE_ SELECT	2	Signal to switch between various ENOB modes (optional)
GAIN_SELECT	2	Select the full-scale input range (0.8V, 1.0V or 1.2V)
DATA_OUT	12	Digital output signal, unsigned binary
DATA_READY	1	Indicates that the conversion is complete and the output is updated. This signal can be used to re-clock the output data.

Table 2: port function description

Detailed description

The converter is active when the power_down and reset signals are both disabled. When the start signal appears, the conversion starts by taking a sample of the input signal, as shown in Figure 2. When the conversion is finished,

the digital data appears at the output and the data_ready signal gives a pulse that can be used to re-clock the output data.
The ADC core requires a clock frequency (f_{CLK}) of 18·f_S. The input impedance of the ADC is purely capacitive, since at the end of the conversion the charge on the capacitors is restored before the sample-switches are re-activated.

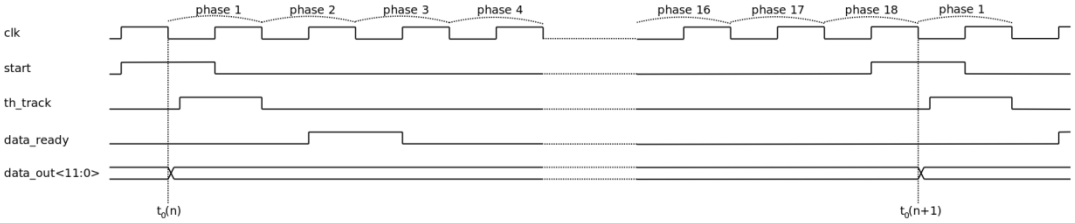

Figure 2: Timing diagram of the ADC

Figure 3 shows the SNR as a function of the input power for the three different settings of the full-scale voltage. For the 0.6V gain setting and low input powers, the dynamic range (DR) is 67 dB and for full-scale signals the SNR is 63 dB. For 0.5V and 0.4V gain settings, the DR is 1 dB, respectively 2 dB less, due to the reduced input power.

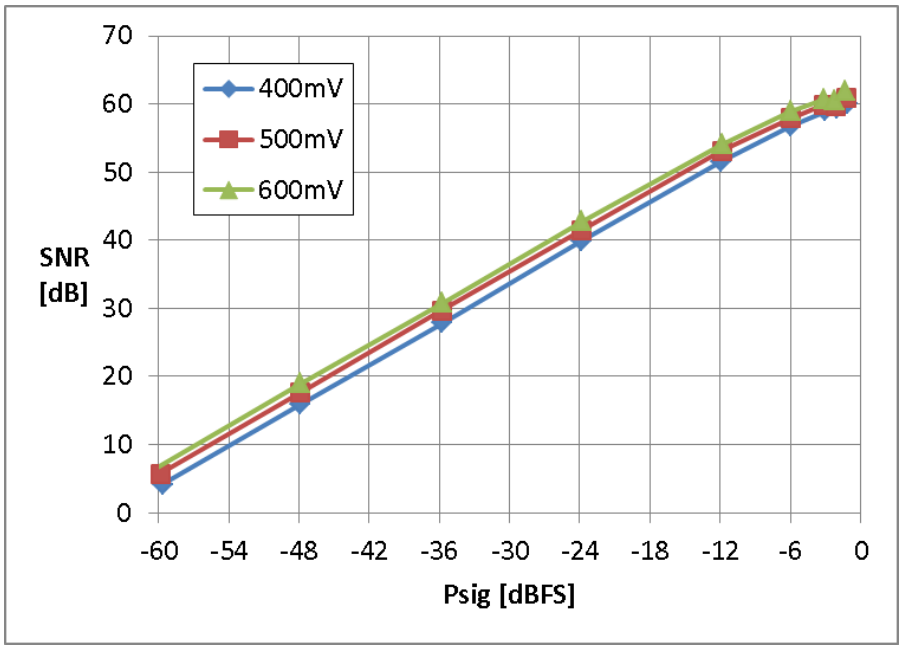

Figure 3: SNR as a function of the input power for the three different settings of the full-scale voltage

Deliverables

The IP deliverables consist of a GDS file, a behavioral model, a netlist and integration documentation. The product can be delivered as a single IP component for customer integration or Axiom IC engineers can integrate the product as part of a SoC engagement.

Options

For generating a bandgap reference voltage suitable for the ADC (programmable from 0.4V to 0.6V), Axiom IC offers an energy-efficient bandgap reference specifically aimed at this converter and adjustable to the customer's requirements. Multiple ADCs can be used with a single bandgap reference in a time-interleaved ADC.

The converter can be extended with gain and/or offset calibration.

For additional information, please contact us at info.enschede@teledyne.com.

Revision history

The following table lists the revision history, only major revisions are shown.

Revision	Date	Reason for revision
F3	2017-07-18	Template update
F2	2012-06-05	Included measurement results, updated description
F1	2012-04-16	Initial version based on SAADC10MS12b

Table 3: Document revision history

For more information about Teledyne DALSA visit our Web Site at

http://www.teledynedalsa.com/semi/mixed-signal/

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