AXIOM_PULLFIRDAC

High Accuracy Low OOBN ΣΔ DAC

Features

- Dynamic range: 117 dB (20 - 20kHz)
- Excellent THD performance:
  THD < -110 dBFS
- Low out-of-band-noise (OOBN): -60 dBFS
- Good matching properties
- Robust against clock jitter
- Insensitive to inter symbol interference (ISI)
- Multi-bit advantages with a single bit modulator
- Silicon proven in CMOS 0.14 µm
- Differential current outputs
- High output compliance: no direct need for buffer
- Area: 0.75 mm^2 per channel

Applications

- High accuracy digital-to-analog conversion with low OOBN
- Signal generation for class-D and class-AB amplifiers
- Audio subsystem
- Makes a complete audio front-end system in combination with up-sampling filters and digital audio interface

Description

The AXIOM_PULLFIRDAC is a high accuracy sigma-delta digital-to-analog converter. The low out-of-band-noise (OOBN) down to -60dBFS makes the converter ideally suited for application with strict OOBN requirements. The PWM modulator is a special type of 1-bit sigma-delta modulator that produces a pulse width modulated (PWM) signal with a fixed repetition frequency. A fixed repetition rate makes the output signal insensitive to non-linear inter symbol interference (ISI).

The semi-digital FIR filter topology of the FIRDAC makes the FIRDAC behave as a multi-bit DAC. This gives the converter its excellent OOBN and makes the system robust against clock jitter and other error sources typically associated with 1-bit converters while maintaining excellent THD and good matching properties.
The AXIOM_PULLFIRDAC is ideally suited for digital-to-analog conversion in front of (analog) class-D or class-AB amplifiers. In addition this IP is delivered together with up-sampling / interpolation filters as signal pre-processing. The design and layout of the FIRDAC is a highly automated process, easy to scale and good portable to several CMOS technologies.

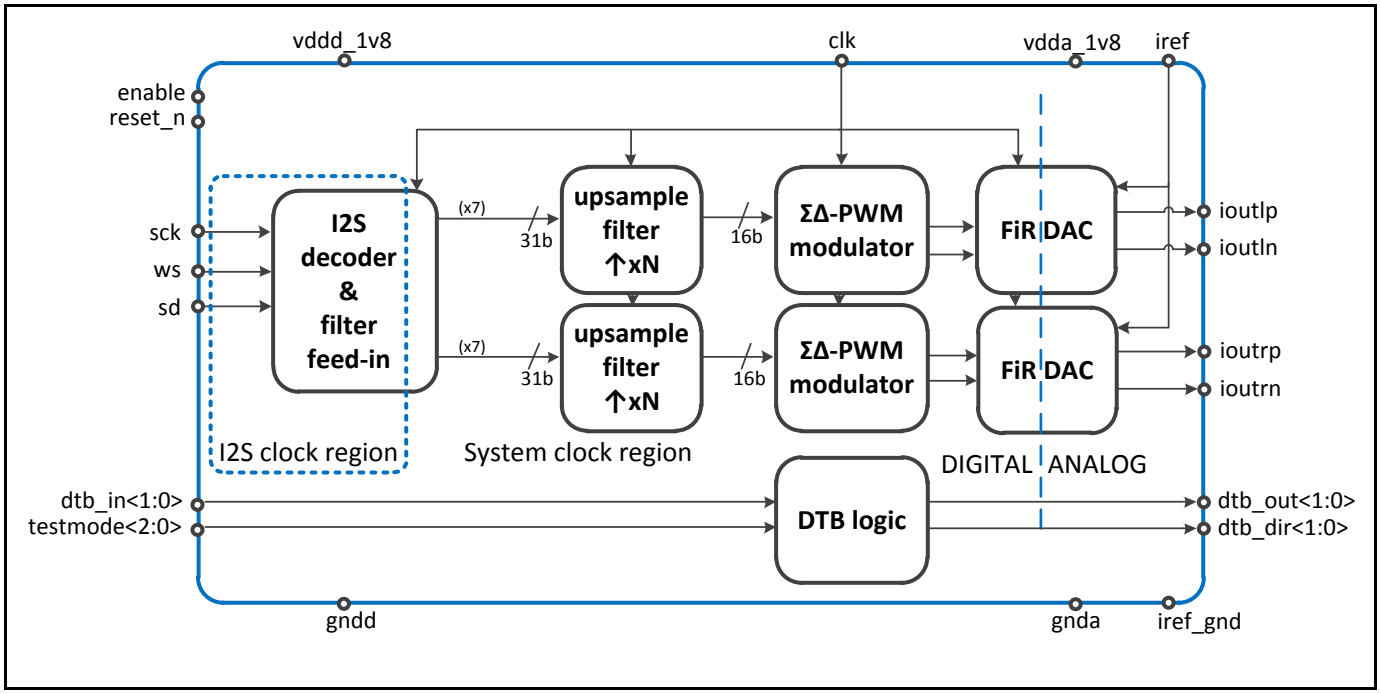

Figure 1 – Block diagram of the FIRDAC IP

Specifications

Default test conditions

Supply voltage (V_{DDA} & V_{DDD})	1.8 V
Reference voltage (V_{OUTCM})	1.6 V
Sample rate (f_S)	96 kHz
Ambient temperature (T)	25 °C

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
TECHNOLOGY					
XFAB XP018	0.18µm CMOS technology, options: Low Power 1.8V 5.0 Volt MOS 3 Thin Metals Top & Thick Metal:METTP & METTPL TECH CODE: "1233" PDK version 3.0.2 Corelib version 1.0 Assura version 3.0.3		0.18		µm
Area	Analog area of one channel		0.4		mm^2
	Analog area of two channels including reference diode and decap		1.1		
	Area including two channels, reference diode, digital modulator and interpolation filter		1.5		
TEMPERATURE					
T_{OP}	Functional operating temperature full performance functional	 0 0	25	 85 125	ºC
ELECTRICAL					
V_{DDA}	Analog supply voltage[1]	1.65	1.8	1.95	V
V_{DDD}	Digital supply voltage[1]	1.65	1.8	1.95	V
I_{PDA}	Power down current[2]		1		µA
I_{PDD}	Power down current[2] [3] [4]		11		nA
$I_{DDA/CH}$	Analog supply current per channel		2.6		mA
$I_{DDD/CH}$	Digital supply current per channel[4] [5]		3.4		mA
$I_{FIRDAC/CH}$	FIRDAC differential signal current	-4.4		4.4	mAp
	FIRDAC single-ended output current[6]	1.0	3.2	5.4	
I_{BIAS}	Reference current input[7]		0.1		mA
V_{OUTCM}	Common mode output voltage	1.2	1.6	1.8	V

[1] Devialet applicates external voltage regulators of (3v3 and) 1v8 to provide the supply for the DAC. The regulator voltage is expected to have a maximum deviation of 5%
[2] Not a key specification to Devialet, could be adjusted if required
[3] Clock inputs clk and sck must be inactive for power-down
[4] Estimated by Cadence Encounter 14.21-s062_1
[5] Analyzed with 192 kHz sample rate. Test signal input for internal net activity estimation : sine wave at 10 kHz with an amplitude of -1.4dBFS.
[6] Preferred output current to match first generation ASIC, higher value than minimal required current
min = I_{REF}*(1-1/BO)/2, typ = I_{REF}/2, max = I_{REF}*(1-(1-1/BO)/2)
[7] Provided by Devialet, requires external filtering to enable SINAD requirements

INPUTS					
f_S	Input sample rate[8]		96 192		kHz
f_{SCK}	I^2S clock frequency f_S = 96kHz f_S = 192kHz		64*f_S 6.144 12.288	 12.5	kHz MHz MHz
f_{CLK}	System clock frequency f_S = 96kHz f_S = 192kHz		256*f_S 24.576 49.152	 50	kHz MHz MHz
f_{PWM}	PWM frequency		f_{CLK}/16		Hz
j_{TOL}	Jitter tolerance[9]			1.5	ns_{RMS}
N	Input data word-length (I^2S)[10]	24	24		bits
PERFORMANCE					
DR	Dynamic Range[11] (20Hz-20kHz,-60dBS input) Un-weighted A-weighted[12]	 116 >116	 117		 dB dBA
$SINAD_{MAX}$ A.K.A. $SNDR_{MAX}$ or -(THD+N)	Signal to Noise And Distortion ratio[13] with 1kHz input Un-weighted A-weighted 10kHz input 100Hz input		 110 >110 110 110		 dB dBA dB dB
OOBN	Integrated out-of-band-noise[14]		-60		dBFS
GD	Digital gain from PCM input to PWM output		-0.27		dB
G	Overall gain from PCM input to DAC output[15]		$6.2/(2^{23}-1)$		mA/LSB
ΔG	Inter-channel gain variation			0.1	dB
BO	Back-off margin[16]	1.13		2.73	dB
X_{TALK}	Channel Crosstalk	-100			dB
R_P	Digital pass-band ripple from 20Hz to 20kHz			0.005	dB
R_F	Overall pass-band roll-off @ DC @ 20kHz, f_S=96kHz @ 40kHz, f_S=96kHz @ 40kHz, f_S=192kHz		 -0.27 -0.77 -2.67 -0.77		 dB

[8] Two input sample rates are supported
[9] Amount of white cycle-to-cycle jitter that gives 3dB decrease of dynamic range
[10] Left-Justified, channel select low = left channel, high = right channel, with one bit-clock delay, see Figure 8
[11] Test condition: SNR measurement with -60dBFS input, integrated noise bandwidth from 20Hz to 20kHz; DR = SNR+60dB.
[12] For this measurement an A-weighting filter has been applied
[13] $SINAD_{MAX}$ is given as the maximum obtainable SINAD for an input frequency of 1kHz
[14] Integrated over a band from 20kHz to 500kHz, Devialet probably will use passive filter as well therefore this isn't a required specification
[15] A 100% modulated PWM output results in 6.4mAp differential output current. The interpolation filter has a gain of -0.27dB so a full scale digital input sinewave has 6.4mA*10^(-0.27/20)= 6.2mA output
[16] Margin required to keep the PWM modulator stable without invoking its limiters limiting performance is -1.4dB. 0.27dB of this margin is already implemented in the interpolation filter gain, the rest of the attenuation needs to be implemented externally by the customer. The BO margin can be increased to e.g. 3dB to trade off higher full-scale performance versus noise performance.

	@ 80kHz, f_S=192kHz		-2.67		
PSR	Power supply rejection[17] (with -60dBFS 1kHz input) 1.5kHz 200mV$_{PP}$ at V$_{DDA}$ 19.5kHz 200mV$_{PP}$ at V$_{DDA}$ 766.5kHz 200mV$_{PP}$ at V$_{DDA}$		 -100 -100 <-110		 dBFS dBFS dBFS

Table 1 – Specifications of the FIRDAC

Port list

Port list of complete system

PORTNAME	WIDTH	DIRECTION	DESCRIPTION
sck	1	input	I²S input: continuous serial clock also referenced as bitclock
ws	1	input	I²S input: word select used to select between left and right channel
sd	1	input	I²S input: serial data representing the audio content
clk	1	input	System clock used for digital processing
ioutlp	1	output	DAC output current (positive side of the differential output of left channel)
ioutln	1	output	DAC output current (negative side of the differential output of left channel)
ioutrp	1	output	DAC output current (positive side of the differential output of right channel)
ioutrn	1	output	DAC output current (negative side of the differential output of right channel)
gnda	1	input	Analog ground
gndd	1	input	Digital ground
vdda_1v8	1	input	1.8V analog supply voltage
vddd_1v8	1	input	1.8V digital supply voltage
iref	1	input	Reference current input for the FIRDAC
iref_gnd	1	output	Reference current source ground pin for external filtering, **not to be connected to other ground potentials like gnda or gndd**
reset_n	1	input	Digital reset signal reset_n = 0: defining a differential zero output reset_n = 1: reading in digital input data (sd)
enable	1	input	Digital input to enable PULLFIRDAC
testmode	3	input	Digital input to enable and select digital test modes routed to DTB see Table 7 for the testmode descriptions
dtb_in[18]	2	input	Digital test bus input, soft pull down expected on external pins
dtb_out[18]	2	output	Digital test bus output, soft pull down expected on external pins
dtb_dir[18]	2	output	Digital signal wires to set the direction of the bi-directional DTB I/O cells: low(0): DTB I/O cell is output high(1): DTB I/O cell is (high-impedance) input

Table 2 – Port function description

- DTB can be used to bypass the PWM modulator and control the FIRDAC switches directly
- ATB is not required on this level, but could be implemented on chip level in order to test and control the reference current (already available with the implemented external filtering of iref and iref_gnd with a 100uF capacitor) and FIRDAC outputs
- Depending on the implementation target of choice some ports can change name or be omitted, current port list assumes ASIC integration of the analog and digital IP

[17] PSR is simulated to be well below these numbers on subblocks. A full toplevel extraction performance simulation is not feasilble to determine the expected PSR. Note that a previous version of the PULLFIRDAC has measured performance at similar levels.
[18] The indices of dtb_in, dtb_out and dtb_dir correspond to each other, e.g. dtb_in[0], dtb_out[0] and dtb_dir[0] connect to a single I/O cell.

Port list of digital part

PORTNAME	WIDTH	DIRECTION	DESCRIPTION
sck	1	input	I²S input: continuous serial clock also referenced as bitclock
ws	1	input	I²S input: word select used to select between left and right channel ws=0: channel 1 (left) ws=1: channel 2 (right)
sd	1	input	I²S input: serial data representing the audio content
clk	1	input	System clock used for digital processing
gndd	1	input	Digital ground
vddd_1v8	1	input	1.8V digital supply voltage
reset_n	1	input	Digital reset signal reset_n = 0: defining a differential zero output reset_n = 1: reading in digital input data (sd)
enable	1	input	Digital input to enable PULLFIRDAC
testmode	3	input	Digital input to enable and select digital test modes routed to DTB see **Error! Reference source not found.** for the testmode descriptions
dtb_in	2	input	Digital test bus input, soft pull down expected on external pins
dac_left_scan	1	input	Non-inverted FIR-chain return (left) connected to analog
dac_left_scan_n	1	input	Inverted FIR-chain return (left) connected to analog
dac_right_scan	1	input	Non-inverted FIR-chain return (right) connected to analog
dac_right_scan_n	1	input	Inverted FIR-chain return (right) connected to analog
pwm_left	1	output	Non-inverted PWM signal for left channel connected to analog
pwm_left_n	1	output	Inverted PWM signal for left channel connected to analog
pwm_right	1	output	Non-inverted PWM signal for right channel connected to analog
pwm_right_n	1	output	Inverted PWM signal for right channel connected to analog
enable_out	1	output	Copy of enable connected to analog
reset_out_n	1	output	Copy of reset_n connected to analog
clk_out	1	output	Copy of clk connected to analog
dtb_out	2	output	Digital test bus output, soft pull down expected on external pins
dtb_dir	2	output	Digital signal wires to set the direction of the bi-directional DTB IO

Table 0-3: Port function description of digital part

Port list of analog part

PORTNAME	WIDTH	DIRECTION	DESCRIPTION
vdda_1v8	1	input	1.8V analog supply voltage
gnda	1	input	Analog ground
data_inlp	1	input	Non-inverted PWM signal for left channel coming from to digital
data_inln	1	input	Inverted PWM signal for left channel coming from to digital
data_inrp	1	input	Non-inverted PWM signal for right channel coming from to digital
data_inrn	1	input	Inverted PWM signal for right channel coming from to digital
iref	1	input	Reference current input for the FIRDAC
iref_gnd	1	output	Reference current source ground pin for external filtering, **not to be connected to other ground potentials like gnda or gndd**
clk	1	input	Clock coming from digital
reset_n	1	input	Digital reset signal coming from digital reset_n = 0: defining a differential zero output reset_n = 1: reading in digital input data (sd)
enable	1	input	analog input to enable PULLFIRDAC coming from digital
ioutlp	1	output	DAC output current (positive side of the differential output of left channel)
ioutln	1	output	DAC output current (negative side of the differential output of left channel)
ioutrp	1	output	DAC output current (positive side of the differential output of right channel)
ioutrn	1	output	DAC output current (negative side of the differential output of right channel)
scan_outlp	1	output	Non-inverted FIR-chain output (left) connected to digital
scan_outln	1	output	Inverted FIR-chain return (left) connected to digital
scan_outrp	1	output	Non-inverted FIR-chain return (right) connected to digital
scan_outrn	1	output	Inverted FIR-chain return (right) connected to digital

Table 0-4: Port function description of analog part

Measured Performance

The following measurements are performed on the previous PULLFIRDAC connected with resistors to the supply used as current to voltage converters. The measurement equipment used is a Rhode & Schwarz UPL audio analyzer. These figures are used only for illustration purposes since the new PULLFIRDAC has improved specifications. When the silicon is characterized these figures will be updated.

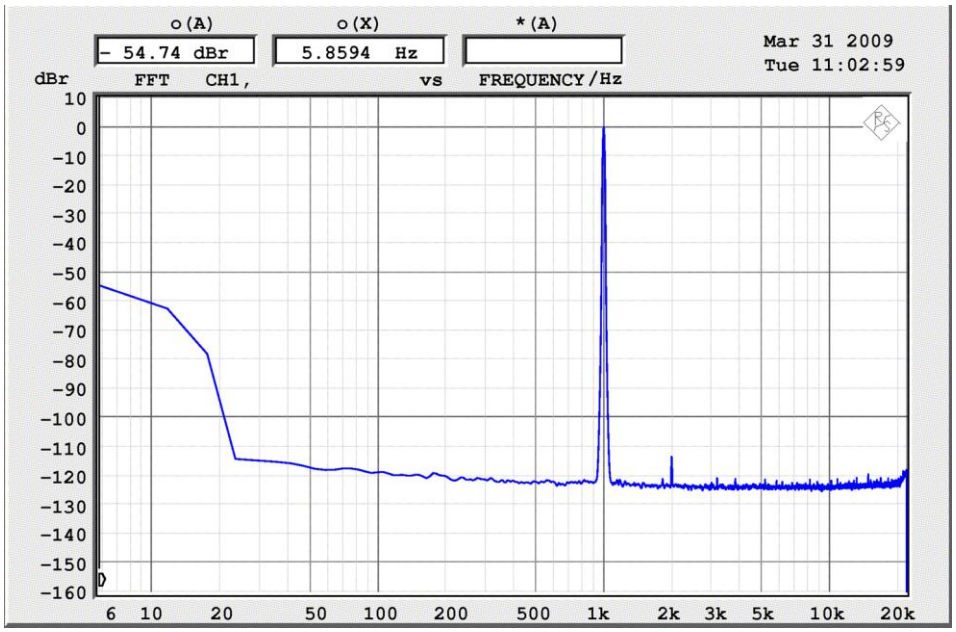

Figure 2 – Output spectrum of the FIRDAC with a single tone @ 1kHz 0dBFS. THD < -110 dBFS.

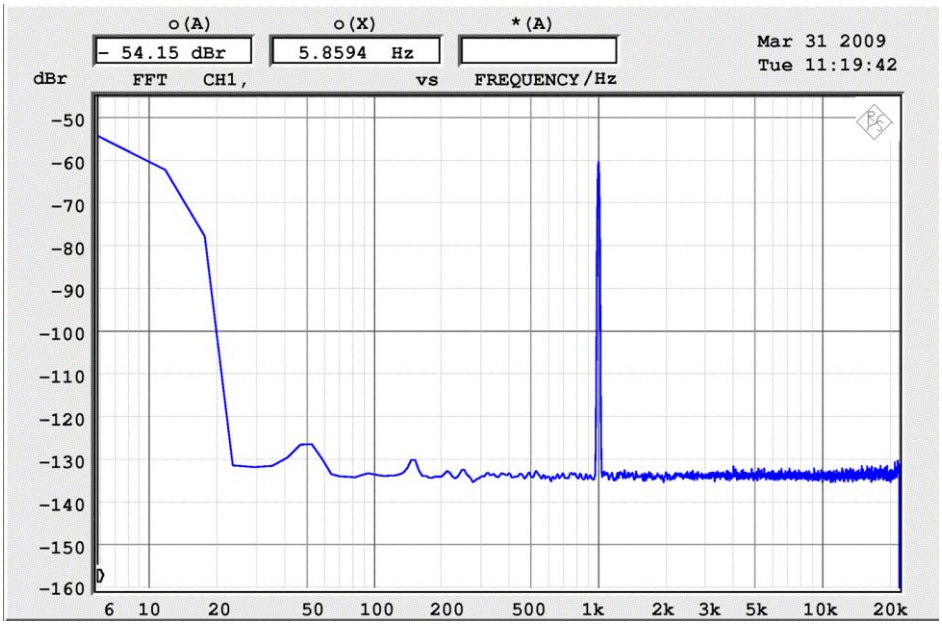

Figure 3 – Output spectrum of the FIRDAC with a single tone of 1kHz

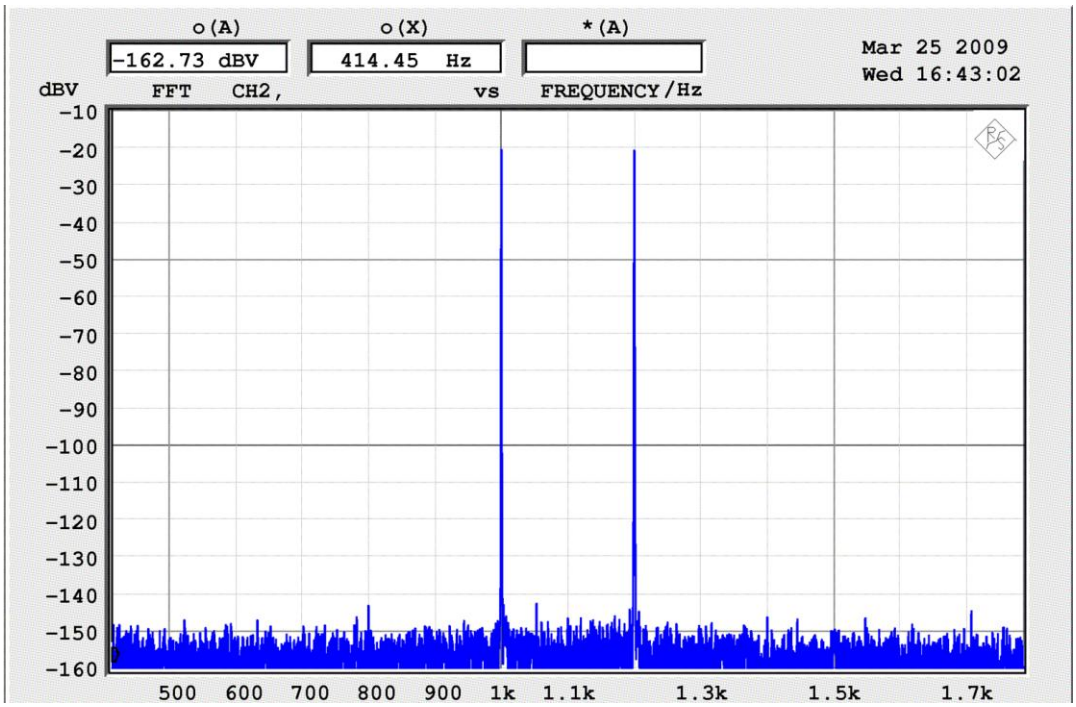

Figure 4 – Two-tone intermodulation 1kHz and 1.2kHz; both input tones at -20dBFS. Intermodulation tone hardly detectable @ 800 Hz.

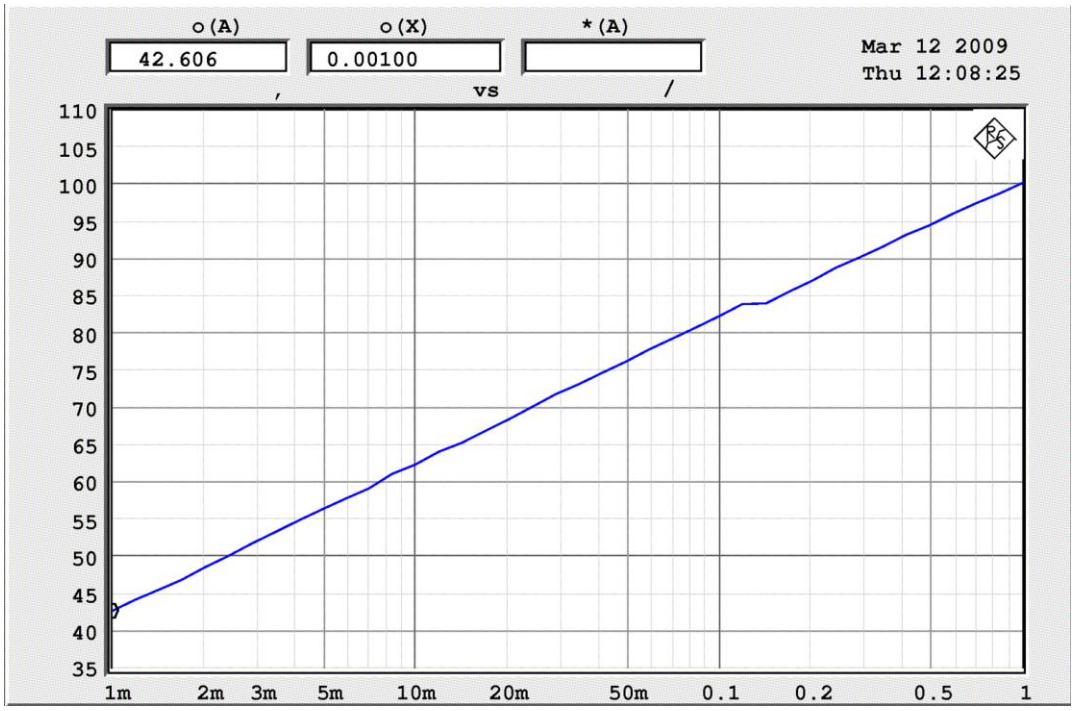

Figure 5 – SINAD vs. input fraction; no weighting filter (irregularity @input 0.12 due to range switching of the audio analyzer)

Application

FIRDAC as input DAC for Devialets ADH® power amplifier

The AXIOM_PULLFIRDAC IP is used for application in the DVT2/ADH2.0 (2nd generation) ASIC of Devialet. It provides a digital input to the ADH® amplifier by means of digital-to-analog conversion. A block schematic overview is shown in Figure 6. The first stage in the signal chain contains a digital serial audio interface, in an I2S-like format. The following digital DAC processing stage contains an IIR filter to up-sample the input from $1f_S$ (96kHz or 192kHz) to the preferred oversampling ratio of $256f_S$ for the 1-bit PWM ΣΔ modulator. The actual D/A conversion takes place at the DAC stage where the FIRDAC converts the PWM signal to a multi-bit like analog signal with build in semi-digital FIR filtering. Volume control and mute can be implemented (by Devialet) on system level.

Advantages compared to traditional converters

Compared to a system with a traditional converter this system comes will the following advantages:

- Low out-of-band noise (OOBN) without the need of a separate low-pass filter due to the low pass filtering nature of the FIRDAC
- Robust against clock jitter and other error sources which are typically associated bit 1-bit converters
- The special type of PWM modulator makes the system insensitive to inter symbol interference (ISI)
- Excellent THD and good matching properties
- Usually 1/f noise of a fixed current source is present in the output or needs to be cancelled by chopping. The FIRDAC inherently has a “chopping-like” behavior because of its switching current sources
- Since both differential input signal and bias signal for the amplifier are controlled by the FIRDAC, pop-free start-up can be simplified.

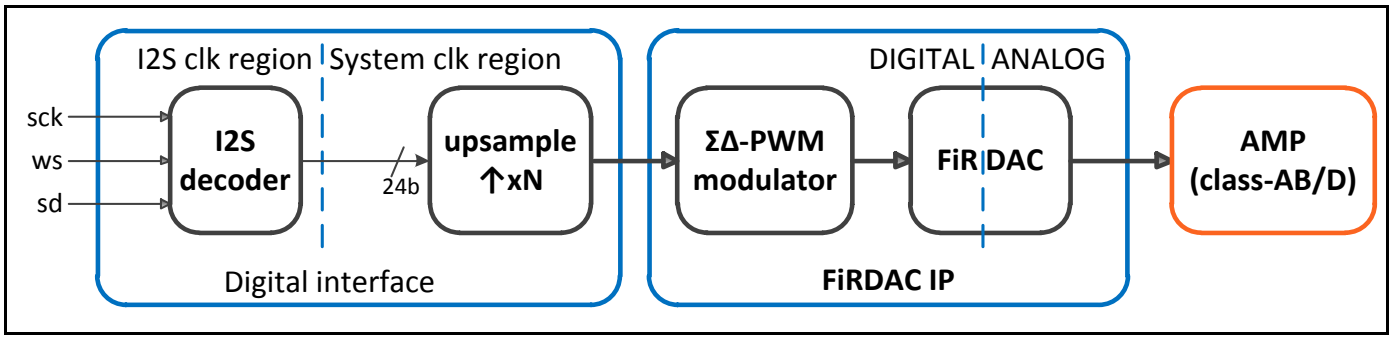

Figure 6 – System overview of the FIRDAC IP for an analog class-D power amplifier

The DAC is to be integrated in the DVT2/ADH2.0 ASIC and is therefore optimized and designed into the input stage of the linear amplifier. In doing so the current consumption is reduced and system level performance boosted with respect to the 1st generation ASIC which used external data converters. Figure 7 shows how the AXIOM_PULLFIRDAC is applicated in the input stage.

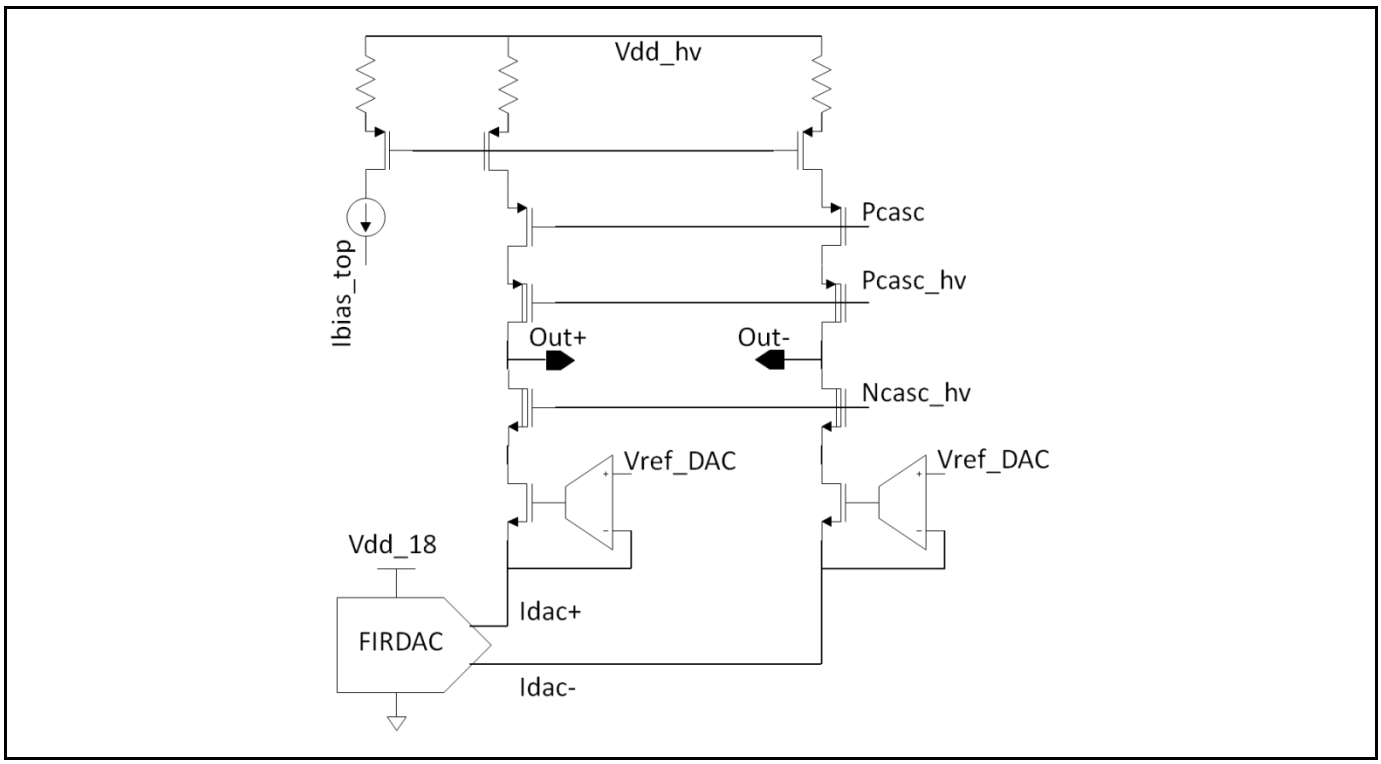

Figure 7 – AXIOM_PULLFIRDAC applicated in the input stage of the linear amplifier

Audio Data Interface

The PULLFIRDAC IP follows a fixed, particular form of the Philips I²S data format [PHIL1986] (see Figure 8), in which the two channels are multiplexed on a single serial line. The interface employs three input signals: sck (bit clock), ws (left/right word select) and sd (serial data). The state of the ws and sd signals is latched internally on the rising edge of sck.

Compared to I²S as defined in the standard [PHIL1986], the following restrictions apply to the data format:

- The PULLFIRDAC acts as a slave, i.e. sck and ws are both inputs
- All words must be at least 24 bits long, but only 24 bits are actually used and additional bits are ignored
- Data words should be left justified, so the MSB is received one sck cycle after a change of ws is received
- A complete frame consists of a left-channel word followed by a right-channel word

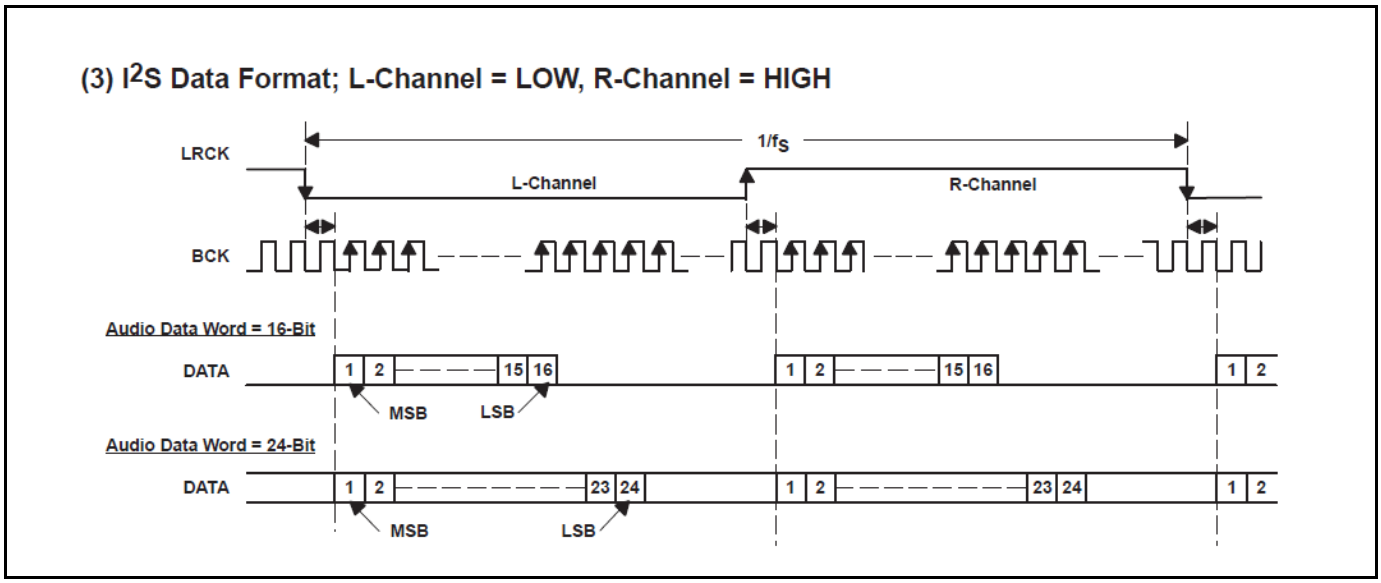

Figure 8 – Audio data interface specification (I²S) [PCM1794A]

Timing quantities for the interface are illustrated in Figure 9 and the allowed values are specified in Table 5.
The I²S bit clock (sck) must be synchronous to the master/system clock (clk), hence the PULLFIRDAC contains a single clock domain. The allowed delay between the two clocks is illustrated in Figure 10 and specified in Table 5.

As is the case for all digital inputs, the internal circuitry connected to the I²S inputs is designed to be driven by the Q output of a BUJILLX1 buffer cell in the X-FAB XP018 technology.

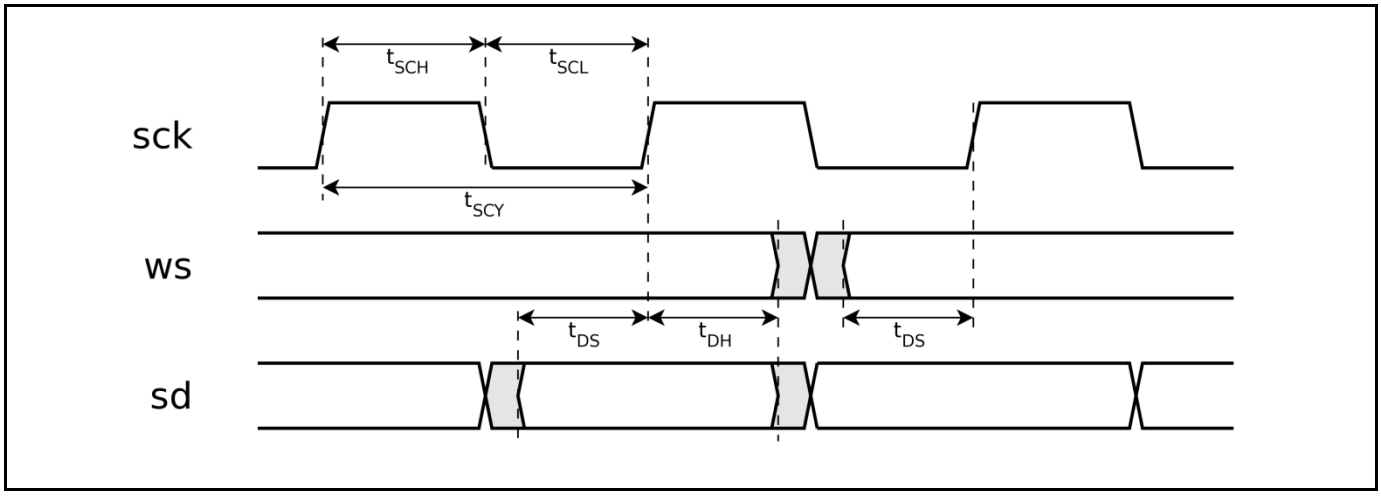

Figure 9 – Audio data interface timing

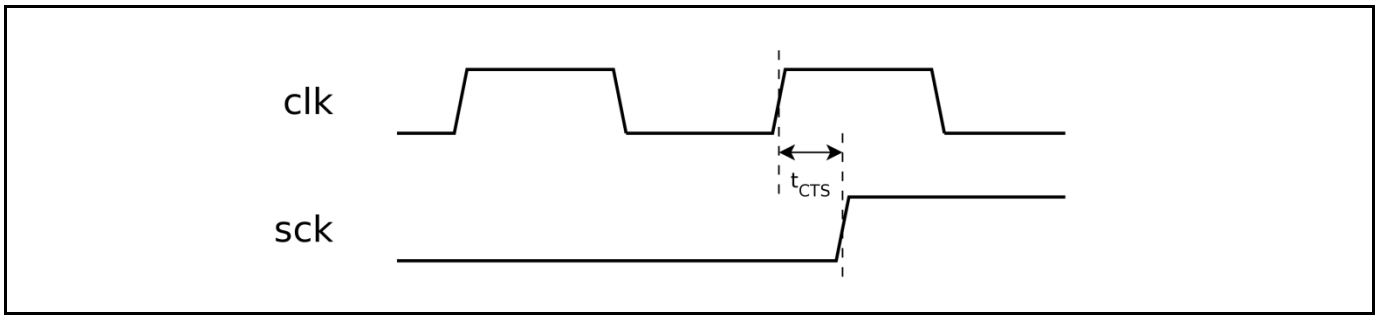

Figure 10 – Definition of clk-to-sck delay

PARAMETER	DESCRIPTION	MIN	MAX	UNITS
t_{SCY}	sck pulse cycle time	80	-	ns
t_{SCL}	sck pulse low duration	40	-	ns
t_{SCH}	sck pulse high duration	40	-	ns
t_{DS}	ws and sd setup time	0.83	-	ns
t_{DH}	ws and sd hold time	1.02	-	ns
t_{CTS}	clk-to-sck delay			
	Worst case[19]	-0.65	15.34	ns
	Typical operating conditions[20]	-0.71	17.47	

Table 5 – Audio data interface timing

[19] V_{DDD} = 1.62V, T = 125°C, slow process corner
[20] V_{DDD} = 1.8V, T = 25°C, typical process corner

Delivery

The IP deliverables consist among other of a GDS file, a RTL code, a behavioral model, a netlist and a datasheet with integration documentation. The product is delivered as two parts. The first part is the GDS2 file that containing the analog toplevel. The second part (digital) is delivered as RTL code and additional a constraint file is added.

VIEW	FILE TYPE	DESCRIPTION
Behavioral model	Verilog-A / Simulink	Behavioral model of the IP which can be used for simulation purposes
Netlist	CDL	Netlist for LVS checks and simulation
Schematic	OA	OpenAccess database with schematics and symbols
Layout	GDS2/OA	Layout database of the analog and digital sections
Abstract	OA	Abstract view with layout boundaries and pinning information
Checks	DRC/LVS/ANT	Verification checks results performed on the layout Sign off tool Assura / PVS (Devialet uses Calibre, XFAB sign off tool seems Assura)
RTL	VHDL	VHDL code
Timing & interface	SDF & .V	Timing details and interface information
Documentation	PDF	Datasheet / specifications / integration information

Table 6 – Deliverables of the IP

Integration requirements

Start-up behavior

To avoid “popping” of the system into which the PULLFIRDAC is integrated, any stage connected to the output of the PULLFIRDAC should be enabled no sooner than 325 cycles of clk after the reset_n input was deasserted or the enable input was asserted (whichever occurred last). Before this, the differential output of the PULLFIRDAC can exhibit small current pulses.

Digital IP

Deliverables

The digital IP is delivered as RTL code. Synthesize and place and route will be done by Devialet since the digital will be added to the digital part of Devialet.

Analog IP

Deliverables

The analog IP will be delivered as GDS2 layout view, which can be included in the toplevel chip design as such. The CDL netlist can be used for LVS checks. The DAC includes dummy cells at the edges in order to be less sensitive to the immediate surroundings of the layout. Nevertheless it is advised to include some kind of shield for isolation at the boundaries as well. This can be included in the IP GDS2 or could be done during integration. For the analog IP the shield is inserted in the IP GDS2. It is advised to shield the capp and capn lines on toplevel from the digital.

Reference input (iref)

The reference input terminal (iref) will be externally filtered with a large capacitor (~100uF) to lower the noise contribution of the bandgap reference. The capacitor has to be placed to isolate and filter the gate-source of the reference diode by connecting to the pins iref and iref_gnd. Note that the iref_gnd node is not to be connected to any other ground potential since it is not supposed to carry any signal. The ESD cell protecting the iref pin is expected to have no ESD series resistance. The possibilities with respect to omitting the ESD series resistance are also discussed with Alexandre Huffenus (Devialet) and Markus Frank (X-FAB). For implementation details is referred to these email conversations. It is also recommended to ask X-FAB (ESD experts) to review the chosen and implemented ESD strategy before tape out and have a close look at the connected analog devices like the reference diode.
In order keep the wiring resistance and the potential pollution of the reference input low it is recommended to place the iref pin close to the IP. In order to minimize the crosstalk from the amplifier outputs to the reference pin (which would cause harmonic

distortion), it is advised to choose the pinout carefully, potentially separate or shield the pins with e.g. ground pins or locate the amplifier output pins symmetrically around the reference pin. A review by Teledyne DALSA of the pinout and in a later stage the toplevel layout is recommended.

Toplevel connections

In Figure 11 the layout of the AXIOM_PULLFIRDAC can be found. The orientation in the database is 90 degrees counter clockwise from this orientation. In that case the left channel is at the top.
In the left and right bottom the outputs can be found in METTPL (highest metal layer). A more detailed view can be found in Figure 12. The outputs are placed in METTPL to get the lowest possible resistance connection to the I/V converter. On both sides of the outputs there is a shielding with ground_ref. If these outputs need to cross other lines at toplevel, it is advised to make a shield in METTP (1 metal layer under METTPL). Furthermore, it is important that the delta resistance between the 2 output lines is as low as possible (ideally 0 Ohm). Delta resistance will introduce ISI. Advised is to connect the feedback connection of the magic-wire, that is controlling the output voltage of the pullfirdac, at the output of the pullfirdac and not at the input side of the I/V converter. This is advised to minimize the influence of the output line resistance on the THD.

For lowering the noise contribution of the bandgap reference an external capacitance is used. The capacitance connections are made in multiple metal layers to get a low ohmic connecting to the external capacitance (Figure 12). This capacitance connection to the PAD needs to be the same as in the pullfirdac itself. The Metals used are:

- Capp needs to be connected in METTPL and METTP with a width of 29.1µm.
- Capn needs to be connected in METTPL, METTP and METAL3. Where METAL3 also is used to shield vref (capp). METTPL and METTP width is 10µm, spacing to capp is 3.45µm.

Power connections to PADS needs to be connected in the following metals:

- gnda in METTPL
- vdda_1v8 in METT

The power-supply pins and capp, capn connections are placed 63um more to the inside of the IP-block. This is done to save area on toplevel. With a corner the connections can be route directly to the PADS and therefore the complete AXIOM_PULLFIRDAC can move 63um in the reserved routing area and this will save area on toplevel. This is done on request of Devialet to save area where possible.

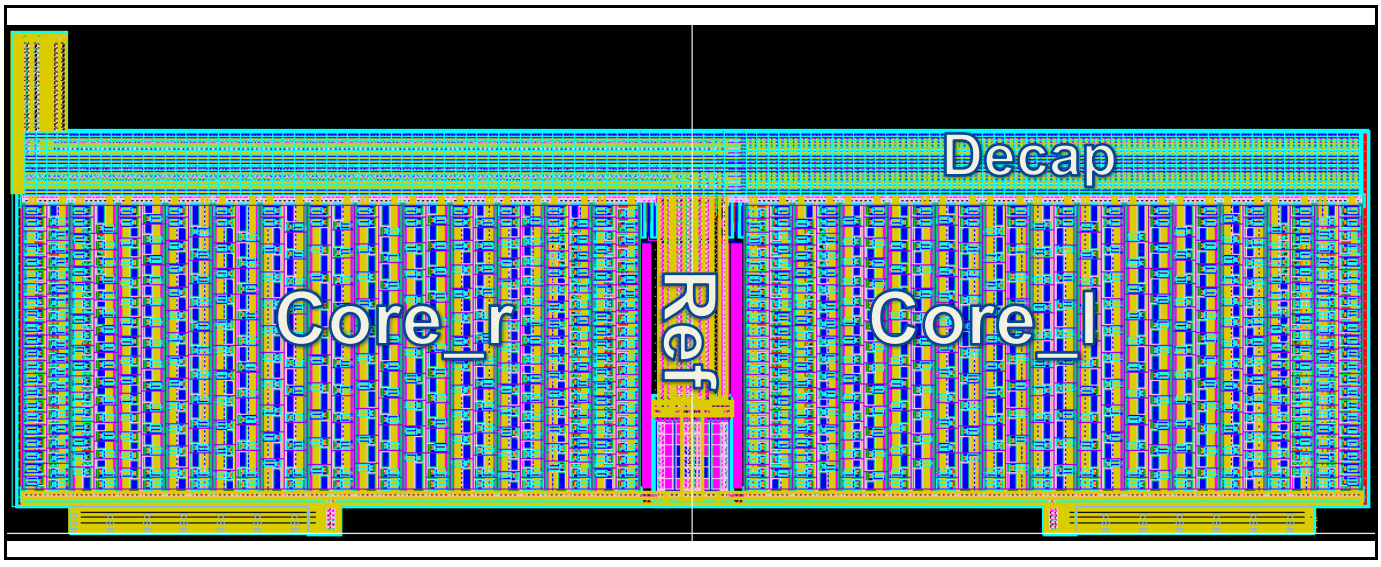

Figure 11 – Layout axiom_xfabxp018_pullfirdac

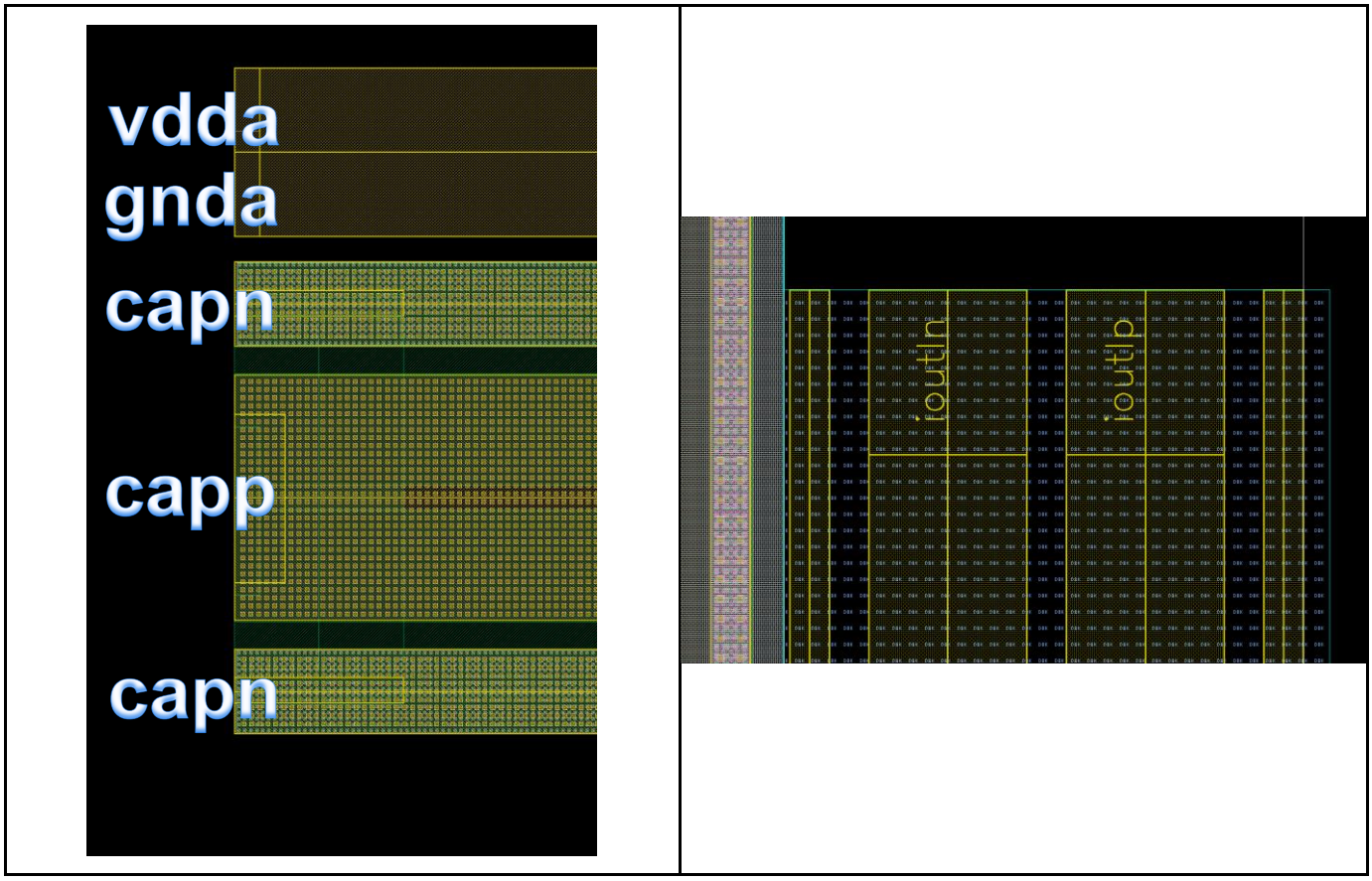

Figure 12 – Layout axiom_xfabxp018_pullfirdac detail view of supply pins and output pins

Physical verification results

Reports of the different runs can be found in the database in the subdirectory assura

DRC results

The following warnings are reported by Assura:

- Bulk should be contacted.

This warning is no issue. The IP makes use of deep-Nwell and therefore the substrate outside the deep-Nwell is not connected. This will be connected on chiplevel. The Pwell in the deep-Nwell of the analog and digital part is connected.

DRC density results

There are no density violations.

For the pullfirdac blocking layers are used. In the complete pullfirdac_ana BlockAll is used.
For the pullfirdac outputs Block METTP & METTPL is used.

LVS results

The following warnings are reported by assura:

- Bulk should be contacted.

This warning is no issue. The IP makes use of Deep-Nwell and therefore the substrate outside the deep-Nwell is not connected. This will be connected on chiplevel. The Pwell in the deep-Nwell of the analog and digital part is connected.

Testability

TESTMODE BITS<2:0>	TESTMODE NAME	DTB_DIR BITS<1:0>	DTB DIRECTION	DESCRIPTION
000	normal operation	11	high-Z	Default setting of testmode<2:0>: testmode disabled, DTB IO could be high-Z
001	modulator bypass mono	11	input	mono mode of operation, both channels receive identical inputs dtb_in_0 → data_inlp & data_inrp dtb_in_1 → data_inln & data_inrn
010	modulator out	00	output	SD-PWM modulator stereo output routed to dtb_out pwm_out_l →dtb_out_0 pwm_out_r →dtb_out_1
011	modulator bypass stereo	11	input	stereo mode of operation, data_inxn follows !data_inxp dtb_in_0 → data_inlp dtb_in_1 → data_inrp
100	scan out stereo	00	output	FIR Filter stereo output routed to dtb_out scan_outlp →dtb_out_0 scan_outrp →dtb_out_1
101	scan out left	00	output	FIR Filter left output routed to dtb_out scan_outlp →dtb_out_0 scan_outln →dtb_out_1
110	scan out right	00	output	FIR Filter right output routed to dtb_out scan_outrp →dtb_out_0 scan_outrn →dtb_out_1
111	Not assigned	11	input	Not assigned

Table 7 – Digital input settings of testmode<2:0> to enable and select digital test modes routed to DTB

This section provides testability suggestions, which can be included in the industrial tests or used for validation purposes. The actual requirements with respect to test coverage and IP validation should be considered on product level in relation to the specific application requirements. Teledyne DALSA can be consulted with testability related questions and could assist in defining specific tests as required.

Test control

Test pins are foreseen on the IP for integration and control on chiplevel.

- The digital test bus (DTB) can be used to control and read out the semi-digital reconstruction filter, which is the last part of the DAC containing the delay line (flipflops) and current sources. For more information on the test modes see Table 7
- As such, a test mode is available to bypass the PWM modulator and control the FIRDAC switches directly, see Table 7
- The DTB can also read out the PWM modulator bitstreams directly
- An analog test bus (ATB) is not required on this level since all relevant signals are available on the interface. An ATB is advised to be implemented on chip level in order to test and control the reference current and FIRDAC outputs directly without going through the power amplifier, but with the current ASIC architecture these nodes are already made available on external pins.

Semi-digital reconstruction filter tests

The semi-digital filter consists of a delay line, built up from flipflops and a number of current sources and switches.

Scan chain tests

The flipflops in the semi-digital reconstruction filter are placed in a delay line configuration. This automatically enables scan chain tests ensuring correct functionality of the flipflops, like scan continuity and stuck-at faults. Although a scan chain test bus is not implemented, similar tests are possible through the DTB.

DAC current sources

The individual DAC current sources could also be tested by using the scan chain controlling the flipflops steering the switches on top of the current sources. This scan chain can be accessed by the DTB (or directly when the digital IP is placed on an FPGA and thus omitted on the ASIC). Tests that can be performed are for example

1. Impulse response test:
   With a lonely one (or a lonely zero) as digital input of the scan chain each current source is sequentially switched towards one of the outputs (depending on the lonely one or zero). The resulting output current at the single ended output (not differentially) will show each individual current source value in time (every clock cycle the next current source is enabled). Basically the impulse response of the FIR-filter is measured during this test. When a current source is faulty this could be detected.
2. Difference test between both channels:
   Since the individual current sources in the FIR-filter, especially the smallest (first and last) coefficients, can be quite small in absolute value it might be better to measure the difference of both channels. If both FIRDACs input signals are inverted and the outputs are shorted, the individual current sources will cancel each other. This way both FIRDAC current sources can be tested at the same time (saving test time by a factor two) and a single comparator or ADC could detect faulty current sources. Without failing taps the mismatch between both FIRDACs is measured at the differential output. With a failing tap the differential output will be much larger and thus easily detected.
3. Thermal noise measurement:
   When an idling bitstream, alternating ones and zeros, is presented at the input of the scan chain the differential output can be measured on thermal noise performance.
4. SINAD / SNR / DR measurements:
   By generating bitstream (e.g. with the PWM modulator in matlab) different input signals can be provided without the use of the actual PWM modulator. When a full scale sine, or a -60dB input sine is applied the performance figures can be measured on the “analog” part of the PULLFIRDAC.

Functional tests

A combined and straight forward way of testing the AXIOM_PULLFIRDAC would be to test the complete signal path, which could even be extended to the complete ASIC.

1. Noise floor measurement:
   Applying zero input to the PULLFIRDAC also enables a noise floor measurement. The thermal noise floor should be low and constant from sample to sample
2. Full scale input measurement:
   Applying the maximum input signal to the PULLFIRDAC enables a SINAD measurement, showing the distortion products

References

[PHIL1986] Philips Semiconductors, “I²S bus specification”, http://en.wikipedia.org/wiki/I%C2%B2S, February 1986

[PCM1794A] Texas Instruments, “PCM1794A, 24bit, 192kHz sampling, advanced segment, audio stereo digital-to-analog converter datasheet”, November 2006

Revision History

REVISION	DATE	REASON FOR REVISION
F1	2014-10-21	First final version accompanying the study report, will be updated during design wrt interfacing when the implementation choice of the digital content is made (FPGA vs. ASIC integration)
F2	2015-03-27	Final version for IP delivery
F3	2015-04-24	Updated final version for IP delivery Updates after internal reviews: Added condition (footnote) on I_{PDD} specification (p2) Added "Estimate by …" footnote on I_{PDD} and I_{DDD} specs (p2) Updated BO specification+footnote (p3) Updated R_P specification (p3) Emphasized operating conditions for requirements on t_{CTS} (p9-10) Added start-up behavior info to integration requirements (p11) Updated Rf specification (p3) and corrected for digital gain, marked other specs that need to be double checked Updated I_{PDA} specification (p2) Added note to PSR (p4)
F4	2015-05-20	Updated t_{CTS} max values (considering clocked delay in clock-crossing circuitry) and description (p9-10)
F5	2016-01-23	Version for second IP delivery. In this version the digital is moved to digital of Devialet and temperature coefficient of the reference diode and output current is improved

Table 8 – Document revision history

For more information about Teledyne DALSA visit our Web Site at

http://www.teledynedalsa.com/semi/mixed-signal/

or contact us at

Teledyne DALSA Enschede
Colosseum 28
7521 PT Enschede
the Netherlands
+31 (0)53-7990700
info.enschede@teledyne.com