Flexible binning structure for CCD color imagers

Jan Bosiers, Harry van Kuijk, Agnes Kleimann, Inge Peters, Frank Polderdijk
DALSA Professional Imaging,
High Tech Campus 27, 5656 AE Eindhoven, The Netherlands
Phone +31-40-259 9016; Fax +31-40-259 9005; E-mail jan.bosiers@dalsa.com

Abstract

We developed a very flexible on-chip horizontal and vertical, RGB-compatible, binning structure for CCD imagers and implemented it in a new 60M-pixel CCD with 6µm x 6µm pixels. The purpose is to allow users of professional digital still cameras with very-high resolution imagers a choice between resolution vs. readout speed and sensitivity. This paper focuses on the design, simulations and measurement results of the on-chip binning structure. The actual binned image configurations that are possible and the result on image quality are not part of the scope of this presentation.

Introduction

A state-of-the art CCD imager for professional digital still camera applications has a typical resolution of around 50M pixels [1], [2]. The full-frame CCD has 6µm x 6µm pixels with an RGB Bayer color filter pattern and on-chip micro-lenses. Four outputs are provided, one each at every corner of the image, each operating at a typical pixel frequency of 20MHz. Fig. 1 shows a typical floor plan. With this configuration the maximum frame rate for a 60M-pixel imager is limited to about 1.1 fps. Higher frame rates require either more parallel outputs, or faster readout speeds per output. However, these options are not desirable from the customer point of view due to increased overall system complexity and cost.

RGB Binning Concept

We therefore developed an on-chip flexible RGB color-compatible binning structure that allows on-chip reduction of both horizontal and vertical resolution while maintaining the RGB color information. In addition, since this real (true) binning is done in the charge domain before charge-to-voltage conversion, it allows the SNR at low light levels to be increased e.g. with a factor of almost 4 for 2x2 binning. Finally, the structure also allows for vertical sub-sampling, which is required to generate preview images at significantly lower resolution but much higher frame rates.

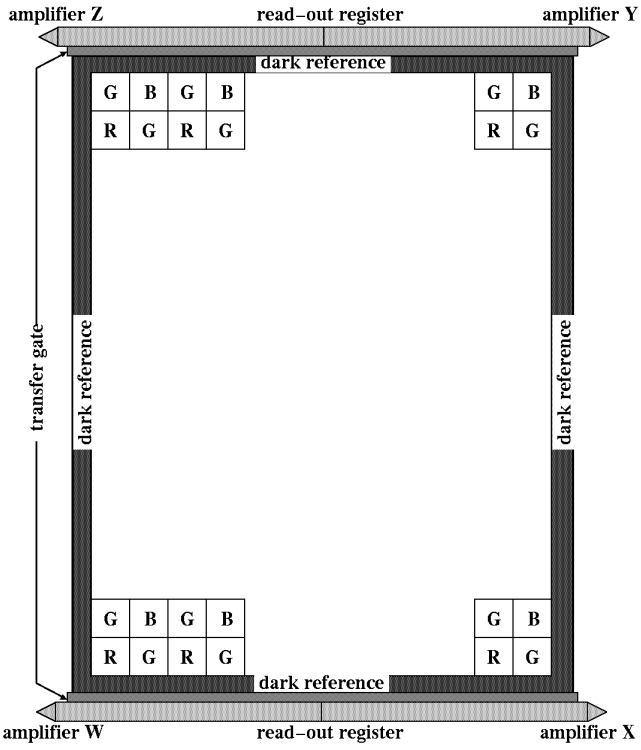

Fig. 1. Typical floor plan of CCD for high-end DSC applications

A schematic representation of the modified sensor design is shown in Fig.2, where a detail of the bottom part of the imager is shown.
Below the conventional readout register, a series of second transfer gates (BTGs) and temporary charge storage cells (STGs) are provided. Note

that in this implementation, the BTGs and STGs are implemented in a four-phase structure (BTG1 and STG1 under columns 1-5-9-…; BTG2 and STG2 under columns 2-6-10-…; etc.). The earlier implementation of charge binning on a 7.2µm x 7.2µm pixel 28M-pixel imager [3] suffered from limited flexibility since only two sets of BTGs and STGs were provided (BTG1- STG1 under columns 1-2; 5-6; 9-10; BTG2 -STG2 under columns 3-4, 7-8, etc).

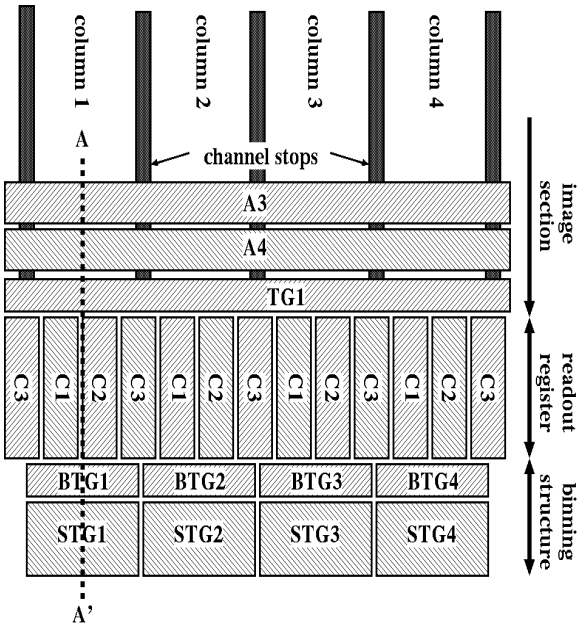

Fig. 2. Design for flexible RGB-compatible binning, showing the additional 4-phase BTG and STG gates

To implement the basic binning scheme as shown on Fig. 3a, presented earlier [3]) as well as more advanced binning schemes (Fig.3b, this work), the design challenges are the following:

- Charge packets have to be moved both to the left and to the right through the horizontal register.
- The horizontal register must have a charge capacity of 2 x the pixel charge capacity.
- Charge packets have to be moved down not only from the image section into the readout register but also down from the image section through the readout register to the STGs; and up again from the STGs back into the readout register.
- With 3 times the pixel charge already under the STGs, it must still be possible to add a fourth pixel charge under STG.
- The STGs need to have a storage capacity of 4 times the pixel charge capacity and must have a 'skimming' mode to reduce their capacity to 1.5…2 x the pixel charge by dumping the excess charge to the substrate.
- The design had to be compatible with the existing flowchart, i.e. no technology changes like additional implants.
- In addition, to support sub-sampling, the design has to support the readout of 2 consecutive lines alternating with the 'dumping' of e.g. 30 lines using the skimming capabilities of the binning structure (2:32 sub-sampling).

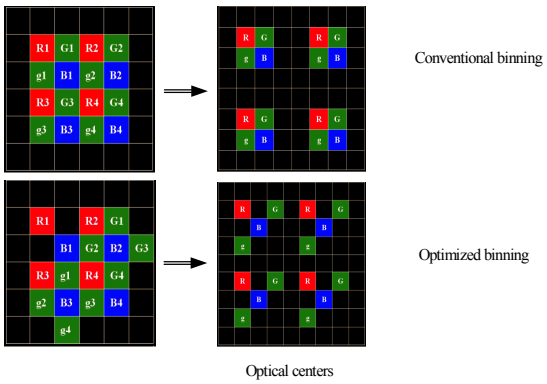

Fig. 3a+b. Result of basic binning
(a) using previous implementation
(b) results of one example of improved binning scheme enabled by new implementation
The left figures show the original pixels that will be binned together, the right figure shows the optical centers of the binned pixels

Device Simulations

Extensive 3-D off-state simulations were performed to ensure efficient charge transport and sufficient charge handling was achieved under all possible conditions. As an example, Fig. 4 shows channel in a cross-section A-A' of Fig. 2, for the transport of 'the last electron' of the 4th charge packet from the image section through the horizontal register to a STG that contains already 4 times the pixel charge. Tapering was applied to the register gates to

increase the electrical field strength in the middle of the wide register (to handle 2x pixel charge), where the fringing fields ("pushing" from TG and "pulling" to BTG) are practically absent. Fig. 5 shows the electrical field at the same location.

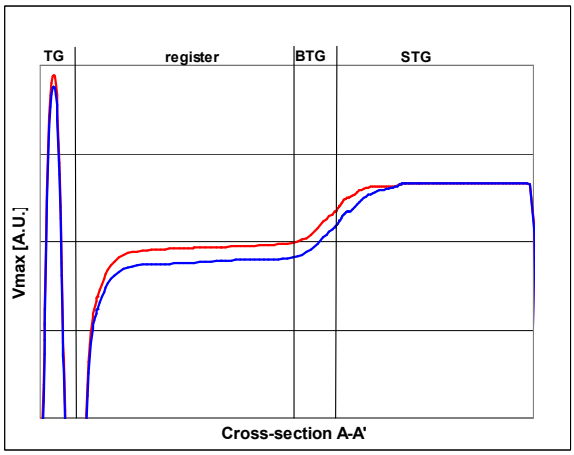

Fig. 4. Channel potential plot along line A-A' of Fig.2 for transport of 'last electron' from register to storage for two values of substrate voltage gates VNS (VNS is adjustable for best anti-blooming)

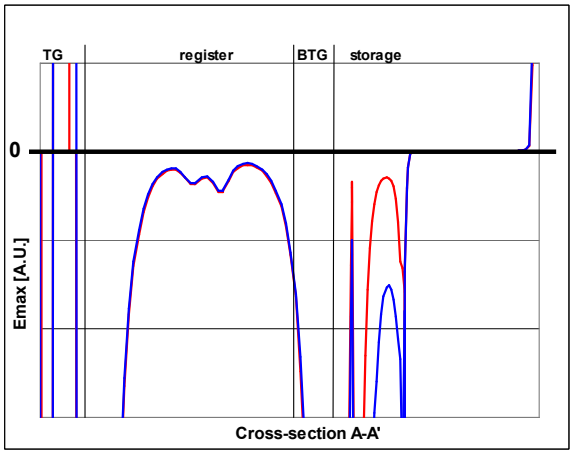

Fig. 5. Electrical field corresponding to Fig. 4, for the same two values of the substrate voltage. The field does not change in polarity (direction) between TG and middle of STG, ensuring a continuous driving field form register to STG

Binning Evaluation

Extensive evaluation of the binning and sub-sampling performance was performed, at 20MHz pixel rate on newly developed 60M-pixel CCD. The results are summarized below:

- Linearity measurements in full-resolution and in 2x2 binning mode. The response of the four color planes R-Gr-Gb-B was measured as a function of exposure time in binning, Fig.6. The linearity plot shows no artifacts, confirming efficient transport of large (blue) and small (green and red) charge packets as well as the functionality of skimming: oversized blue charge packets in saturation are skimmed, without spilling back to the register, and to a sufficiently small size to allow efficient transport through the register.

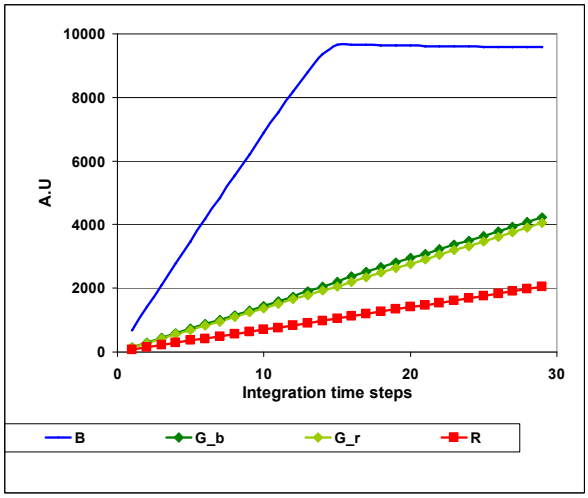

Fig. 6. Response in 2x2 binning mode for the four color planes Blue (B), Green in blue line (Gb), Green in red line (Gr) and Red (R) as function of exposure time for illumination with blue light

- Measurements at low-light levels in binning mode were performed to find the fasted possible transport speeds. Fig.7 shows the situation for correct timing, Fig. 8 shows the onset of incomplete charge transport when the transit times from the register into the storage cells are too short.

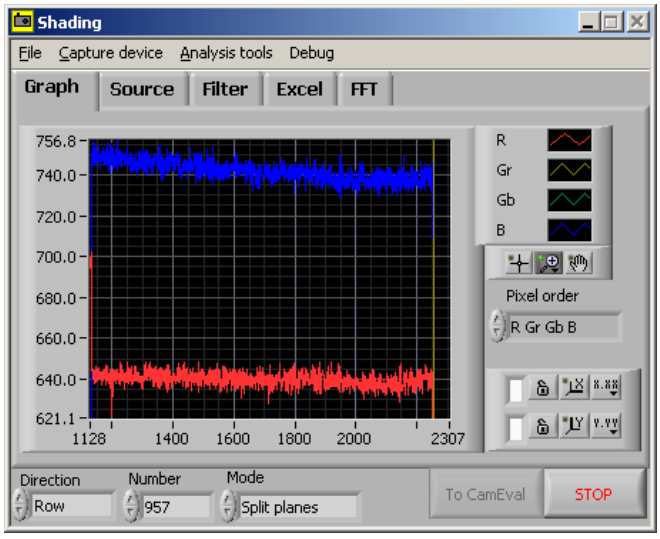

Fig. 7. Blue and red signal from one line readout (green signals are not shown) as function of column position for 2x2 binned pixels for very weak blue illumination for default transport time from register to storage cells.

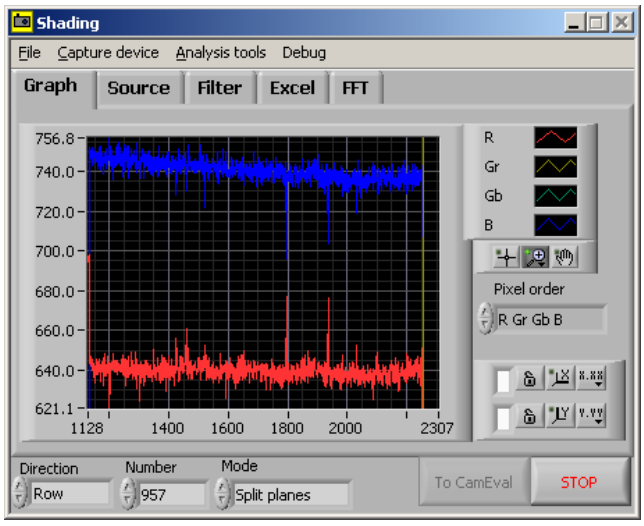

Fig. 8. Blue and red signal from one line readout (green signals are not shown) as function of column position for 2x2 binned pixels for very weak blue illumination for reduced transport time from register to storage cells. Spikes start to occur, showing the onset of incomplete charge transport leading to charge mixing.

Summary and Conclusions

Table 1 summarizes the device performance.

Item	Number	Comment
Resolution	60M	
Pixel Size	6x6μm^2	
Number of outputs	4	Choice to use of 1, 2, or 4
Typical pixel frequency per output	20MHz	
Max. frame rate, 4 outputs	1	At 20MHz per output
Max. frame rate with 2x2 binning, 4 outputs	2.1	At 20MHz per output
Max. frame rate with 2:32 sub-sampling, 4 outputs	6.2	At 20MHz per output
Charge loss during binning	<0.5%	Measurement limit

Table 1. Performance Summary

In conclusion, we developed an improved on-chip RGB binning structure. At 20MHz pixel rate, the frame rate could be increased from 1.1fps to 2.1 fps in the advanced binning mode (Fig.3, bottom), and to 6.2fps in 2:32 vertical sub-sampling mode; without any charge mixing or charge loss, thus ensuring correct color reproduction as with full-resolution images.

Acknowledgements

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References

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