AXIOM_PWMMOD256fs1b

256fs – 1bit PWM sigma-delta modulator

Features

- 117 dB dynamic range
- -120 dBFSA in-band noise
- ISI insensitive bit stream
- No signal dependent kick back on DAC reference
- Multi bit advantages with a single bit modulator
- Hardware costs ~ 700 gates
- 0.018 mm^2 in 0.14µm CMOS
- Silicon proven

Applications

- High accuracy PCM to PWM conversion
- Signal generation for Class-D amplifiers
- D/A converters
- Audio subsystems
- Audio amplifiers with digital inputs
- Ideal in combination with FIRDAC (114dB DR measured)
- FPGA solution with discrete DAC (110dB DR measured)

Description

A PWM sigma-delta modulator is a special type of 1-bit sigma-delta modulator that produces a pulse width modulated (PWM) output signal with a fixed repetition frequency. A fixed repetition frequency makes the output signal insensitive to typical problems associated with (continuous time) sigma-delta converters, such as non-linear inter symbol interference (ISI) and kickback noise on the reference of the DAC.

This IP block implements a digital PWM sigma-delta modulator consisting of a fifth-order loop filter, followed by a 16 taps moving average filter, a sawtooth carrier injection (with a frequency of $f_{CLK}/16$) and a 1-bit quantizer. The functional block diagram is shown in Figure 1.

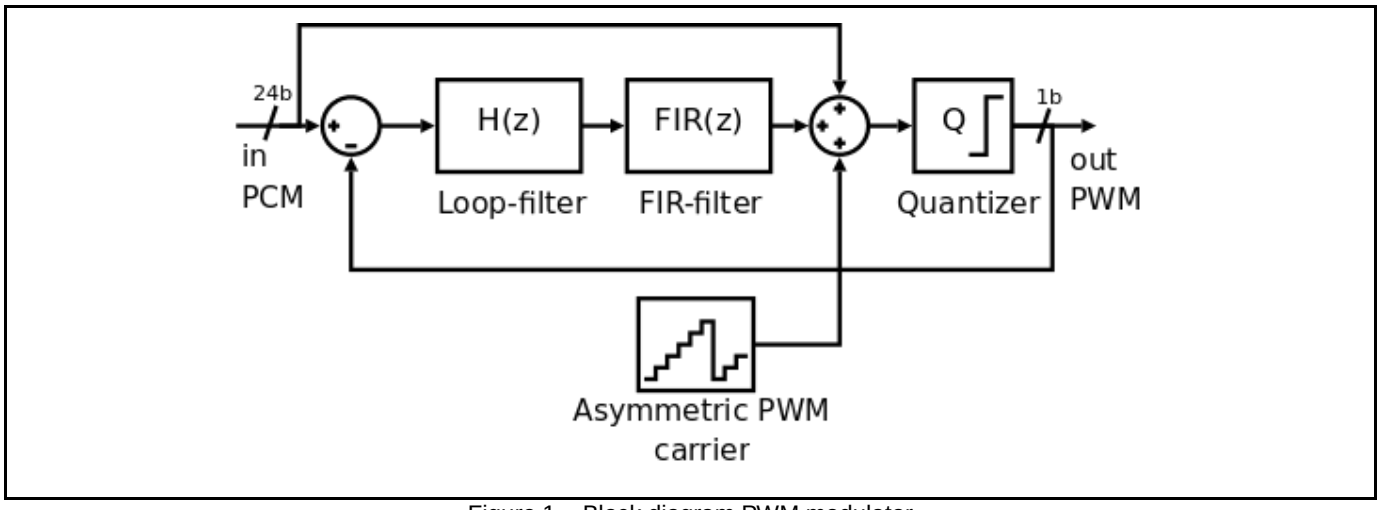

Figure 1 – Block diagram PWM modulator

Proven performance

The PWM ΣΔ modulator was introduced in literature by [DOOR2005]. In that paper, results of a D/A converter show that the PWM ΣΔ modulator enables high audio performance (106dB $SNDR_{MAX}$, 114dB dynamic range, A-weighted) with very simple 1-bit DAC components. That paper also shows that the PWM ΣΔ modulator is very suitable to operate together with a FIRDAC (also known as a 'semi-digital reconstruction filter', see AXIOM_FIRDAC).
In another experiment, with the PWM ΣΔ modulator implemented on an FPGA and a DAC build from common off the shelf (COTS) components (a 74HCT574, 8 resistors, an Op-amp and an RC feedback network), an audio performance of 110dB dynamic range and 97dB $SNDR_{MAX}$ was measured.

Detailed description

A functional block diagram of the PWM ΣΔ modulator is shown in Figure 1. It differs from a standard ΣΔ modulator in two ways:

- A digital 16 step sawtooth is added to the output signal of the loop filter to force a PWM output signal with a fixed switching frequency of $f_{CLK}/16$.
- The loop filter is cascaded with a 16-tap FIR interpolation filter to improve loop stability.

The PWM signal has a 4-bit time resolution, corresponding to 16 discrete pulse widths. With the frequency in the modulator loop being $256*f_S$ this results in a PWM frequency of $16*f_S$. The multi bit behavior of the PWM signal at low frequencies has a positive effect on the loop stability. Therefore, aggressive noise shaping can be used, while the modulator remains inherently stable up to high modulation depths. In this realization with a 5^{th} order loop filter, stable behavior is guaranteed up to 85% modulation depth. A spectrum of the output of the PWM ΣΔ modulator with such an input is shown in Figure 2. As in normal sigma-delta modulators, state limiters inside the loop filter enable 100% modulation depth, but with reduced performance, see Figure 3.

Specifications

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
TECHNOLOGY					
C14	0.14µm CMOS technology		0.14		µm
Area	Chip area in 0.14µm CMOS		0.018		mm^2
N_{GATES}	Number of gates / hardware cost		700		
FREQUENCIES					
f_S	Sample frequency	0	44.1 - 48		kHz
f_{CLK}	Clock frequency (input)		256		f_S
f_{PWM}	PWM frequency		1/16		f_{CLK}
MODULATOR PERFORMANCE					
BW_{PASS}	Stopband edge for quantization noise		0.45		f_S
e_{NQ}	Inband quantization noise of the modulator		-116 -120		dBFS dBFSA
DR	Dynamic range		117		dB
SNR_{MAX}	Maximum Signal to Noise Ratio		116		dB
$U_{IN,MAX}$	Maximum input without invoking limiters		-1.4		dBFS

Table 1 – Specifications of the PWM ΣΔ modulator.

Port list

PORT NAME	WIDTH	DECRIPTION
Clk	1	Clock input, at 256*fs
Reset_N	1	Reset input (active low), resets all states to initial condition
PCM_in	24	PCM input, at N*fs (as long as N*fs is synchronous to Clk)
PWM_out	1	PWM output

Table 2 – Port function description

Typical characteristics

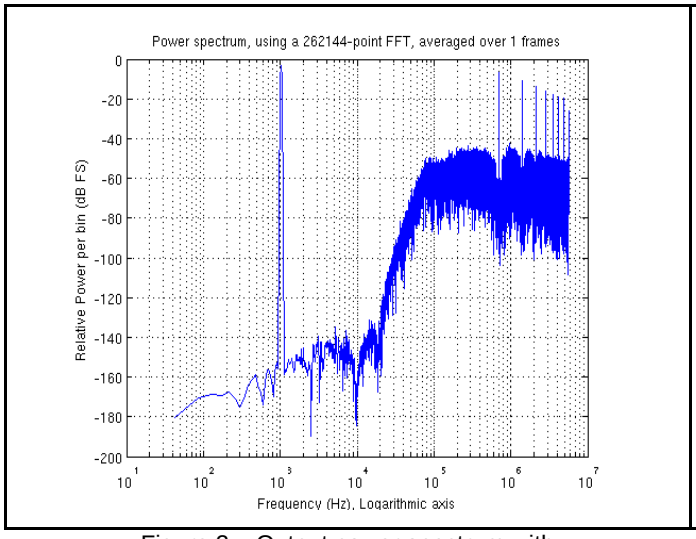

Figure 2 – Output power spectrum with -1.4dBFS input and f_S=44.1kHz.

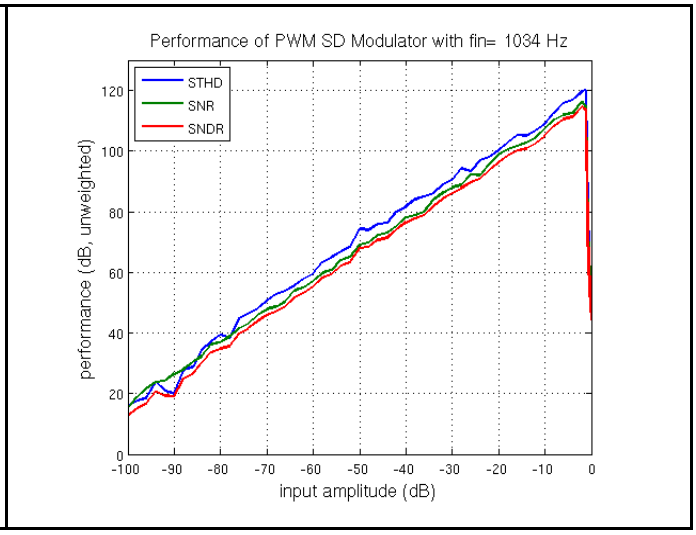

Figure 3 - Modulator performance with f_S=44.1kHz.

Deliverables

The IP deliverable consists of a RTL description in VHDL of the PWM sigma-delta modulator. The product can be delivered as a single IP component for customer integration or Axiom IC engineers can integrate the product as part of a SoC engagement.

Design unit PWM_SD_Modulator (RTL, containing entity and architecture)
File name pwm_sd_modulator.vhd
Version 1.31F or higher
Target Synthesizable as ASIC logic or on FPGA
Limitations None known
Errors None known

Dependencies 1. IEEE.Numeric_Std
2. DSP_functions (package that contains general arithmetic routines, will also be delivered)

Behavioral modeling: RTL code is suitable for behavioral simulations, other types of behavioral models can be delivered upon request.
Samples: bit stream examples are available for experimentation.

References

[DOOR2005] T. S. Doorn, A.J.M. van Tuijl, D. Schinkel, A.J. Annema, M. Berkhout, B. Nauta, “An audio FIR-DAC in a BCD process for high power Class-D amplifiers,” Proc. 31th ESSCIRC, pp. 459-462, Sept. 2005.

Revision history

REVISON	DATE	REASON FOR REVISION
F4	2014-10-08	Initial version in Teledyne template; port from old datasheet format
D5a	2014-12-04	Corrected header, logos, last page links

Table 3 – Document revision history

For more information about Teledyne DALSA visit our Web Site at

http://www.teledynedalsa.com/semi/mixed-signal/

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