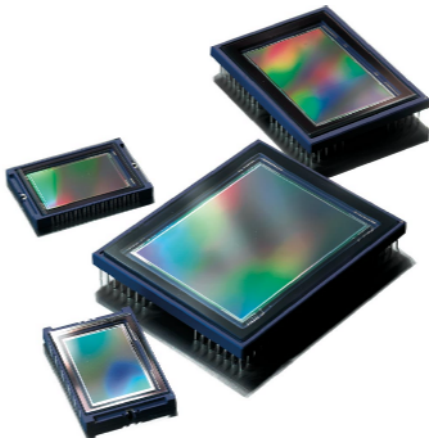
APPLICATION NOTE



Application Note AN09

- FTF2020 CCD Image Sensor
- FTF3020 CCD Image Sensor
- FTF7040 CCD Image Sensor
- FTF2416 CCD Image Sensor
- FTF4027 CCD Image Sensor
- FTF4052 CCD Image Sensor
- FTF5033 CCD Image Sensor
- FTF5066 CCD Image Sensor
- FTF6146 CCD Image Sensor
- SAA8103 Pulse Pattern Generator
- TDA9991 Vertical Driver
- AD9824 Analog-to-digital interface for CCD cameras

April, 2008

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Summary

This application note describes the circuitry to design a 14-bit Digital Still Camera (DSC).
Besides some CCD theory also the peripheral IC's will be discussed.
To get the best picture-performance the guidelines described in this document have to be followed.
Changes made in the described circuitry may degrade the picture performance.

Chapter 1 contains some general information.

Chapter 2, 3 and 4 provide the reader with some basic CCD theory plus some specific details regarding the FTF2020, FTF3020, FTF7040, FTF2416, FTF4027, FTF4052, FTF5033, FTF5066 and FTF6146 CCD.

Chapter 5 presents all of the aspects of the SAA8103, the Pulse Pattern Generator. Basic application diagrams are discussed.

Chapter 6 presents all of the aspects of the TDA9991, the Vertical Driver. Basic application diagrams are discussed.

Chapter 7 presents all of the aspects of the AD9824, a 14 bit analog-to-digital converter. Basic application diagrams are discussed.

Chapter 8 shows an example of the power-management in the DSC- camera

Chapter 9 and 10 summarize all critical issues of the camera design.

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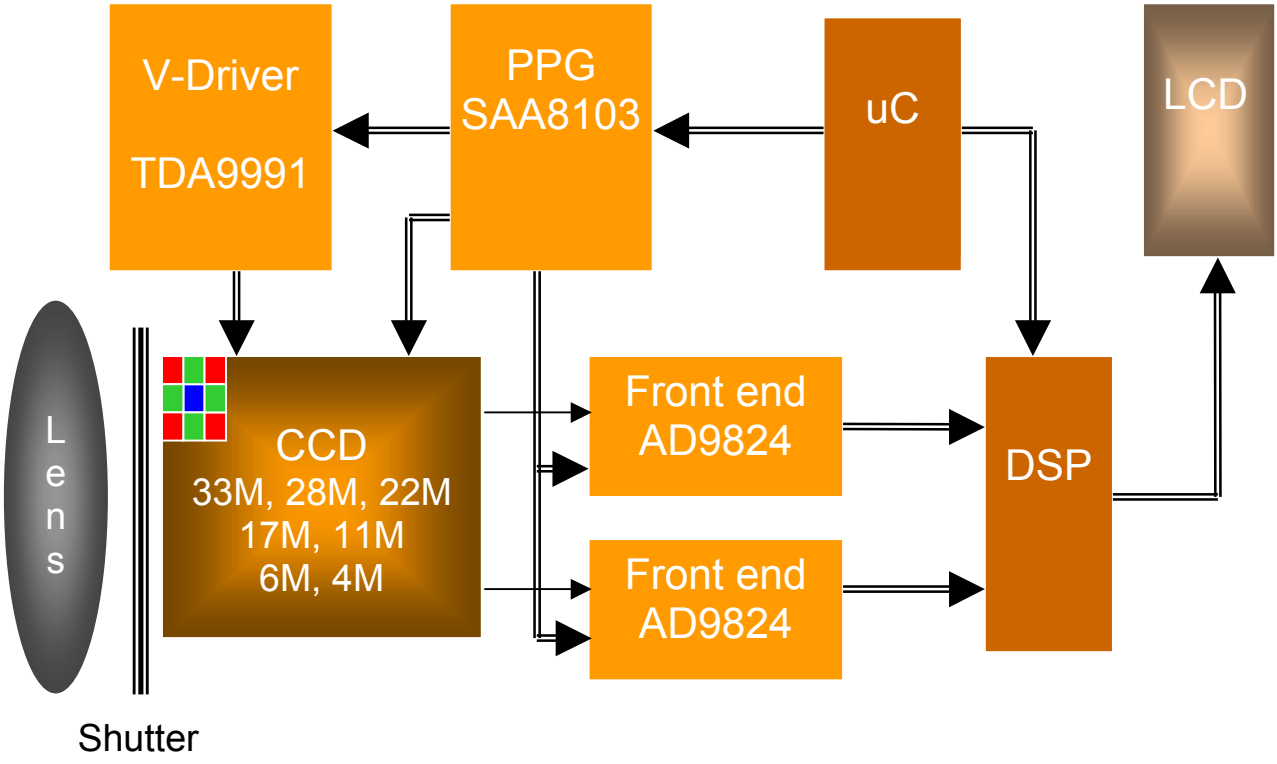
Figures

1. General

This document contains information for camera applications with DALSA area CCD sensors, SAA8103 (PPG), TDA9991 (vertical driver) and AD9824 (analog-to-digital interface for CCD camera's). This note describes the sub-system for a 4, 6, 11, 17, 22, 28, and 33-Megapixel Digital Still Camera in single or dual operation mode. The circuitry described in this note is not yet optimized for low cost mass production. The application note can also be used for several other applications besides digital still.

1.1. Block diagram of Digital Still Camera



2. Sensor operating voltages

To operate the CCD several bias voltages and clocking voltages are necessary. Here is a description on these voltages:

VNS: Voltage connected to the n-substrate of the CCD. The range is between 20 ~ 28V. VNS controls the high-light behavior (anti-blooming) of the CCD. To perform Charge Reset, a CR_pulse is added on VNS. This Charge Reset (also called electronic shutter) is used to remove all charge from the CCD (necessary at the start of a new integration cycle).

SFD: This DC-voltage is connected to the output amplifier of the CCD.

RD: This DC-voltage is connected to the Reset Fet.

RG: This high frequency clock is used to reset the Reset Fet. This reset is necessary for removing the charge from the Floating Diffusion capacitance. Clock frequency is 25MHz.

C1 ~ C3: These three (high frequency) horizontal clocks transport the charge towards the output amplifier. Clock frequency is 25MHz.

SG: This high frequency clock is the last gate before the output gate. The phase of SG is equal to the phase of C3. Clockfrequency is 25 MHz.

A1 ~ A4: The image gates clocks to collect and transport charge in the image array.

OG: The Output Gate is the gate between SG and floating diffusion (see 2.2).

VPS: Voltage connected to p-doped substrate.

BTG1/2, STG1/2 (FTF6146 only): These gates are reserved for future use.

		Unit	FTF2416	FTF4027 FTF4052	FTF2020 FTF3020 FTF7040	FTF5033 FTF5066 FTF6146
Nsub	DC-level	[V]	20-28 *)	20-28 *)	20-28 *)	20-28 *)
CR	Amplitude	[V]	5	5	10	5
	Low level	[V]	VNS	VNS	VNS	VNS
SFD	DC-level	[V]	20	20	20	20
RD	DC-level	[V]	20	20	15.5	20
RG	Amplitude	[V]	5	5	10	5
	Low level	[V]	17	17	5	17
	Frequency	[MHz]	25	25	25	25
C1-C3	Amplitude	[V]	5	5	5	5
	Low level	[V]	3	3	3.5	3.5
	Frequency	[MHz]	25	25	25	25
SG	Amplitude	[V]	5	5	10	5
	Low level	[V]	5	4.5	3.5	4.5

		Unit	FTF2416	FTF4027 FTF4052	FTF2020 FTF3020 FTF7040	FTF5033 FTF5066 FTF6146
	Frequency	[MHz]	25	25	25 (FTF3020, FTF2020) 10 (FTF7040)	25
A1-A4	Amplitude during integration	[V]	8	8	8	8
	Amplitude during vertical transport	[V]	11	11	11	11
	Vertical transport frequency	[KHz]	75	50	50 (FTF3020) 125 (FTF2020) 20 (FTF7040)	50
OG	DC-level	[V]	5	5	6.5	5
Psub	DC-level	[V]	6	6	3	6
BTG1/2 **)						GND
STG1/2 **)						

*) VNS might differ from batch to batch.

**) Only for FTF6146

Please check datasheets on DALSA website for latest sensor voltages.

2.1. Physical Gate Layout

For a better understanding of the sensor operation and the pulse patterns to be used, a schematic overview of the gates of the image and readout sections of the DALSA area CCD sensors is shown.

2.1.1. FTF2020 / FTF3020 / FTF7040 gate layout

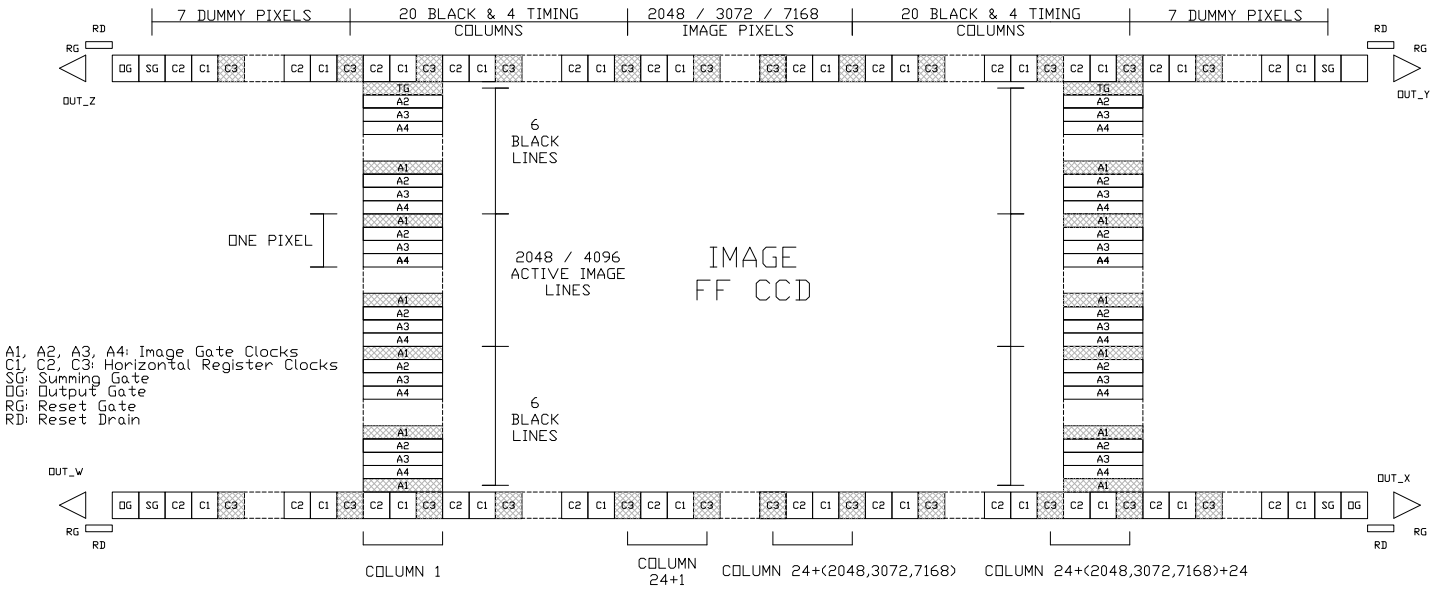


Figure 1: Physical Gate Layout FTF2020 /FTF3020/FTF7040

2.1.2. FTF2416 gate layout

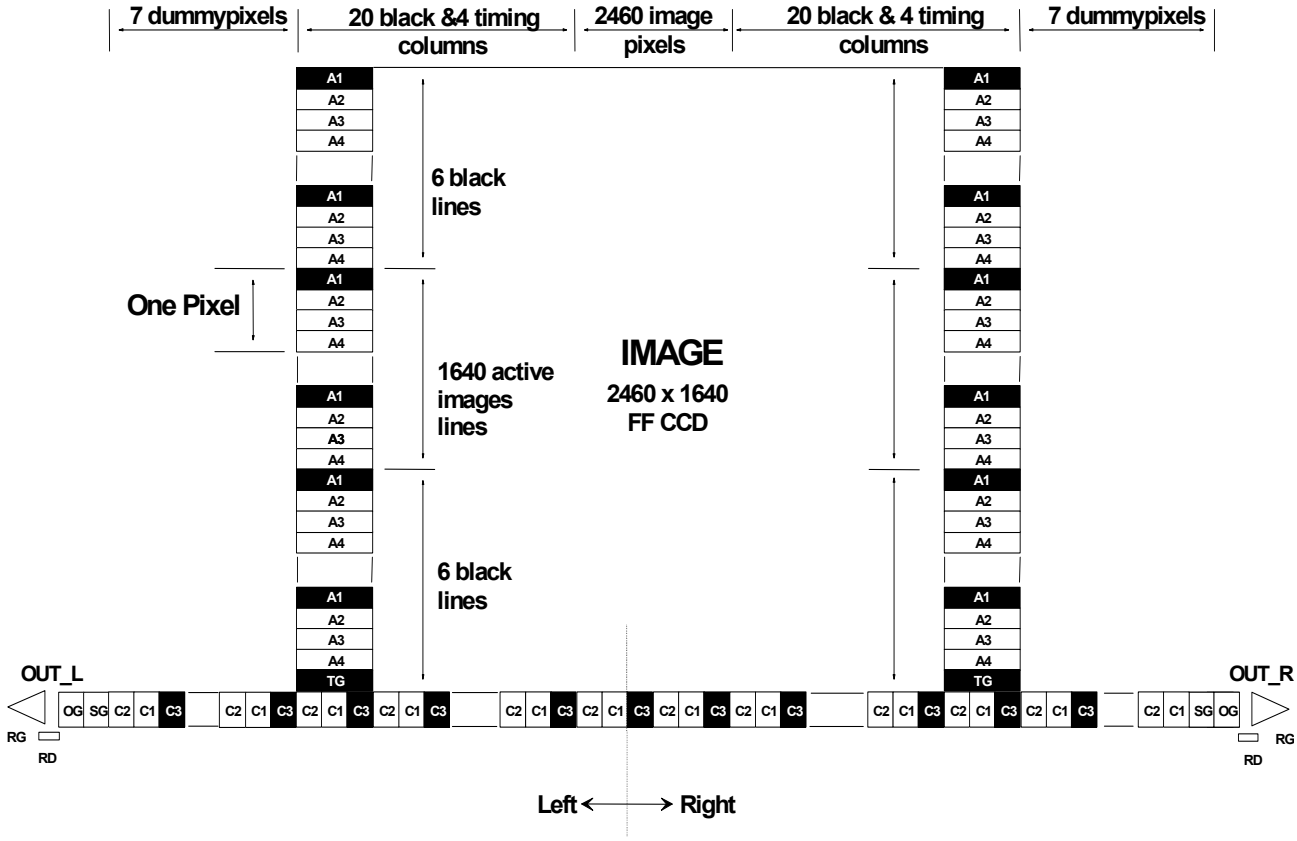


Figure 2: Physical Gate Layout FTF2416

2.1.3. FTF4027 / FTF4052 gate layout

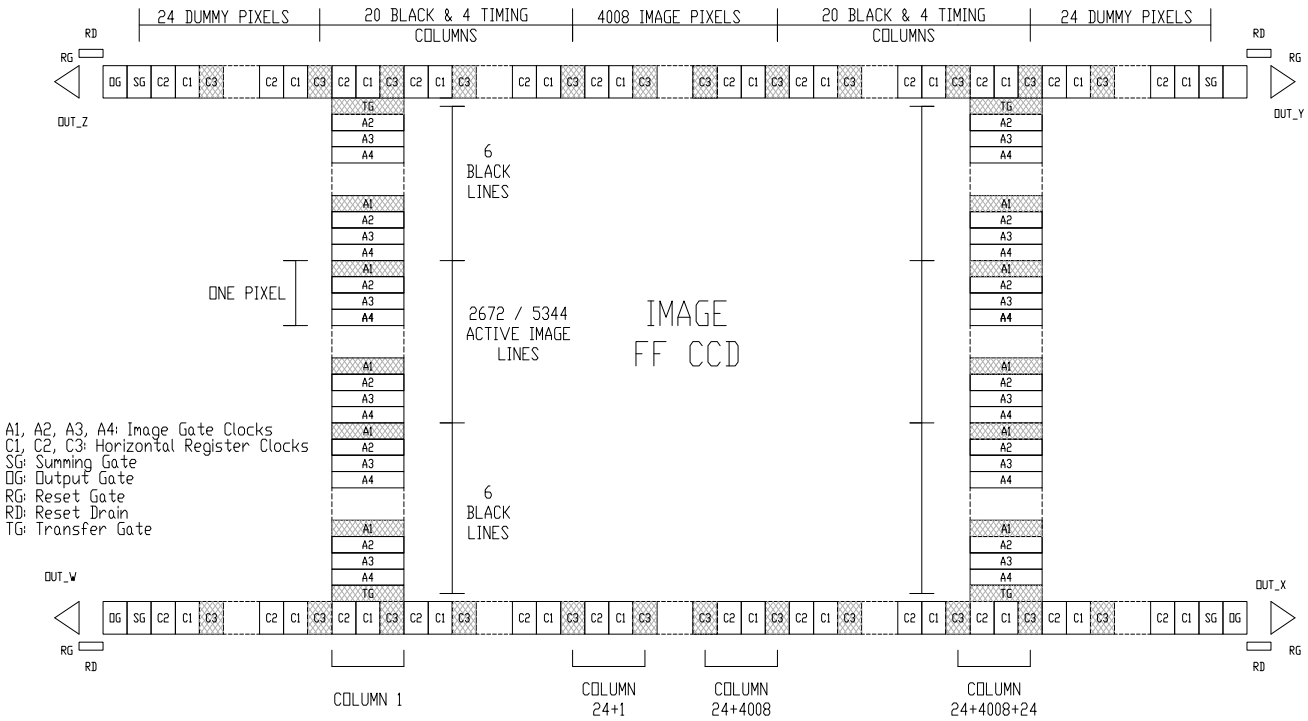


Figure 3: Physical Gate Layout FTF4027 /FTF4052

2.1.4. FTF5033 / FTF5066 gate layout

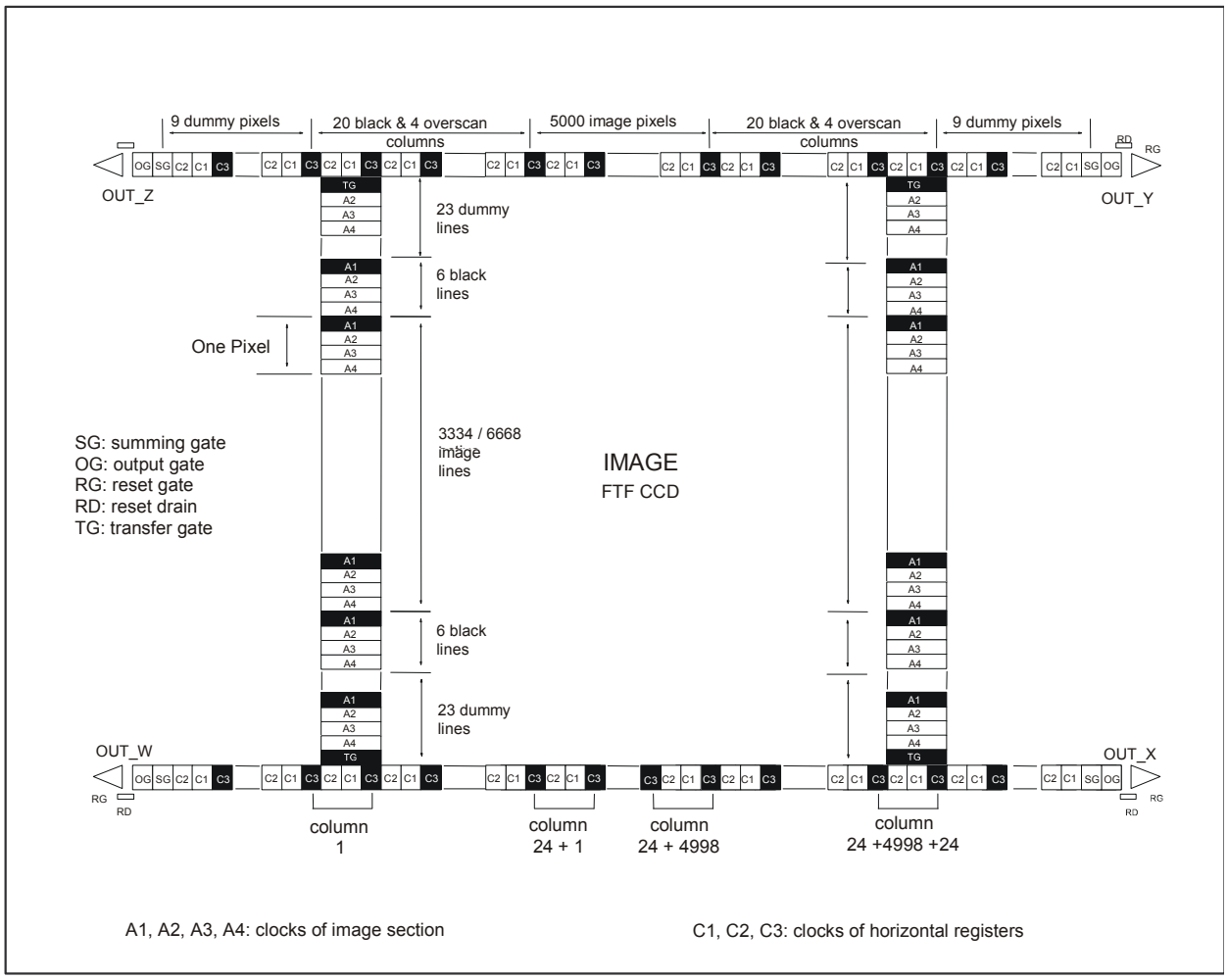


Figure 4: Physical Gate Layout FTF5033 /FTF5066

2.1.5. FTF6146 gate layout

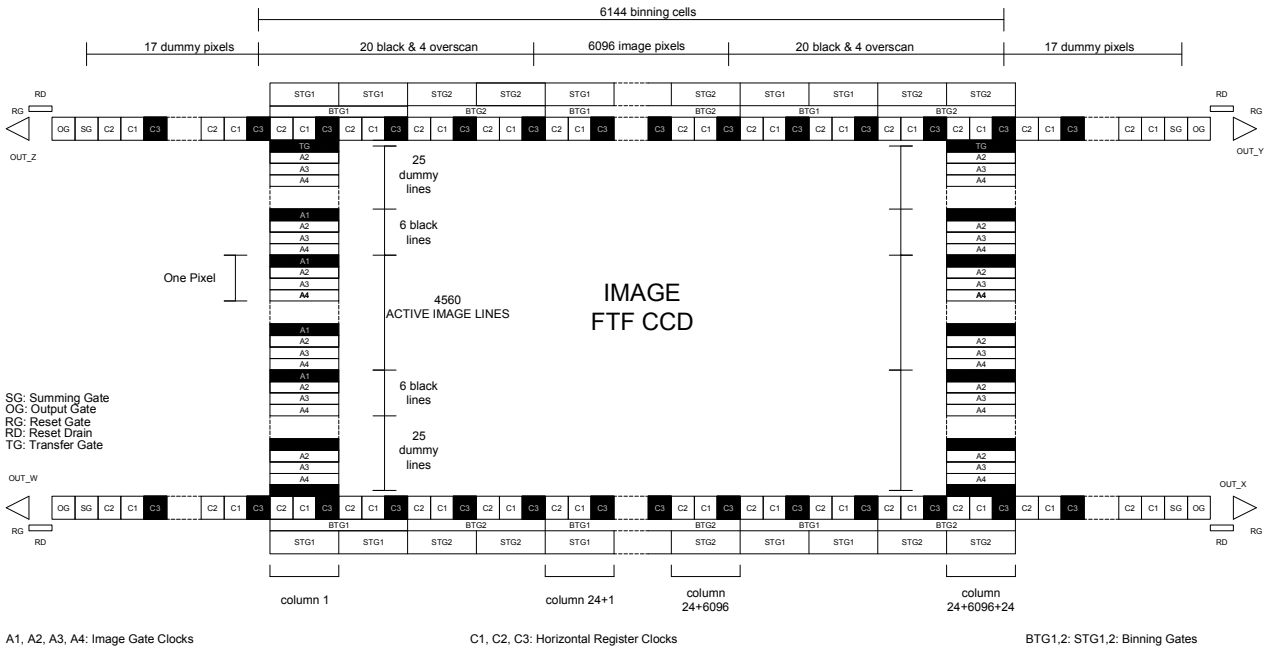


Figure 5: Physical Gate Layout FTF6146

The image pixels are bounded by striped channel-stop implants (p-doped) in horizontal direction and by biasing one of the image gates (A1) at a low (zero) DC-level and three gates (A2, A3, A4) at a high DC-level (8V) in vertical direction. Under image gates A2, A3 and A4, the charge generated by the photons is collected.

2.2. Output Buffer

All of the sensors do have a 3-stage source-follower output buffer, shown in Figure 6. Charge is transported to the Floating Diffusion (FD) from the last serial gate (SG) and output gate (OG). FD is the n-region of a reverse biased diode to VPS with a very low capacitance that converts the charge to a voltage swing. The voltage swing on FD is buffered by three source-follower amplifiers SF1, SF2 and SF3 to the output node. CS1 and CS2 are on-chip current source loads for SF1 and SF2. Source Follower Drain (SFD) is the output buffer positive supply, Source Follower Source (SFS) is the negative supply, Voltage Current Source (VCS) is the gate supply of CS2, both should be connected to analog ground.

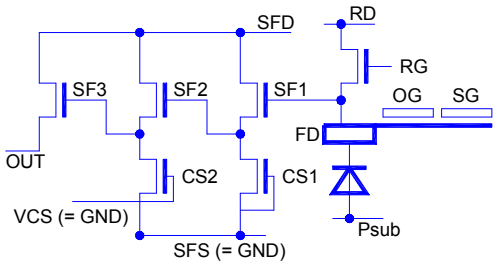


Figure 6: On-Chip Amplifier Circuit

After detection, the FD node is reset (emptied of signal electrons) by applying the reset pulse to Reset Gate (RG), thus resetting the FD potential to Reset Drain voltage RD. SF3 is set by loading the output with an external resistor. The current through SF3 determines the bandwidth of the amplifier. A load of 3.3kΩ allows 25 MHz readout.

3. Sensor Operation

3.1. Number of pixels and lines

	FTF2020	FTF3020	FTF7040	FTF2416	FTF4027	FTF4052	FTF5033	FTF5066	FTF6146
Active pixels per line	2048	3072	7168	2460	4008	4008	4992	4992	6096
Timing pixels per line	2x4	2x4	2x4	2x4	2x4	2x4	2x4	2x4	2x4
Black pixels per line	2x20	2x20	2x20	2x20	2x20	2x20	2x20	2x20	2x20
Dummy pixels per line	7	7	7	7	24	24	9	9	17
Active lines per frame	2048	2048	4096	1640	2672	5344	3334	6668	4560
Black lines per frame	2x6	2x6	2x6	2x6	2x6	2x6	2x6	2x6	2x6
Dummy lines							2x23	2x23	2x25

3.2. Gates

The image gates (A) are designed as four-phase structures, to be driven with 4-phase clocks. The image gates are designated A1...A4.

TG is an image gate which is designed for vertical subsampling for the FTF2416, FTF4027, FTF4052, FTF5033, FTF5066 and FTF6146. In normal operation mode TG should be driven with the same pulsepattern as image clock A1.

Phases A2, A3, and A4 are 'high' during charge integration. Phase A1 is low during integration. Typical clock swing during integration is from 0V to 8V. During vertical transport the clock swing is from 0V to 11V.

STG1/2 and BTG1/2 are reserved for future use with the FTF6146.

The horizontal gates are designed as a three-phase structure. During transport of one line from image to horizontal register gates C1 and C2 should be 'high' while C3 is 'low'. Typical clock swing is from 4V to 9V.

3.3. Waveforms

Figure 3 shows the conventional 4-phase waveform of the vertical image clocks during vertical transport of one line. This means that for 5 units the pulse is high and for three units it is low. The delay from one to the next pulse is 2 units.

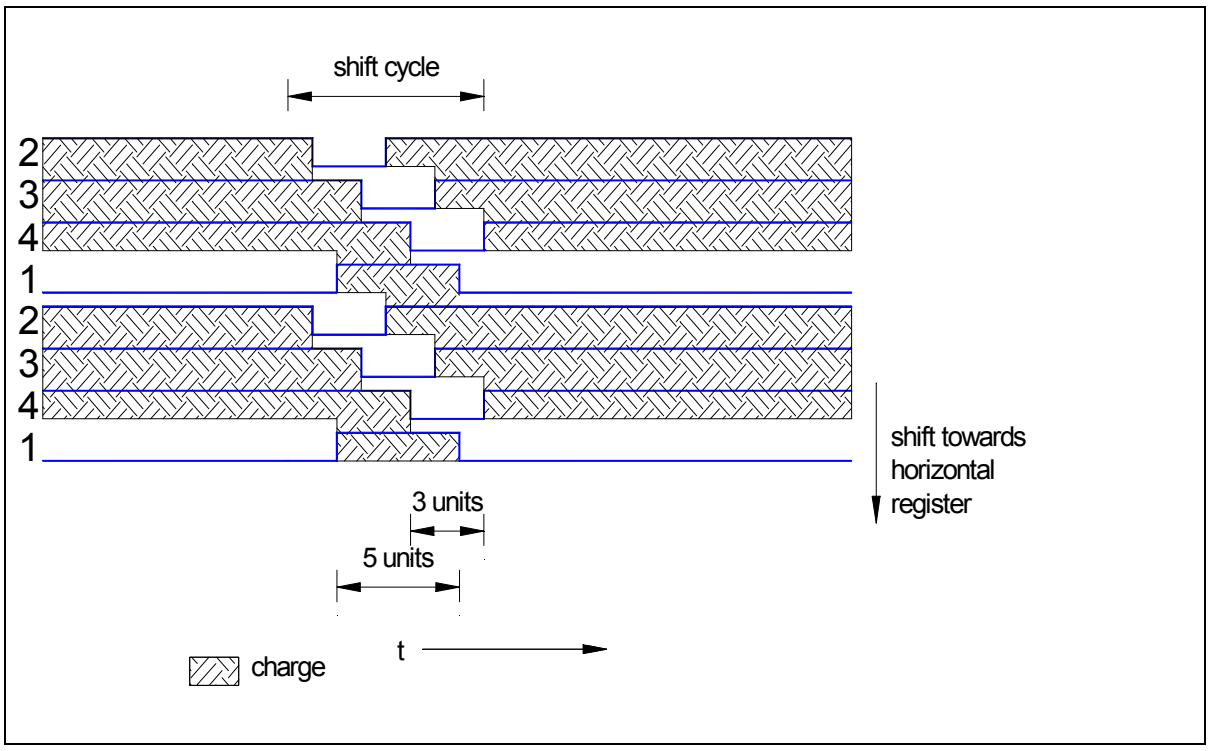


Figure 7: Waveforms during Line Shift

During Integration three Image-gates are kept high.

The most important issue of charge transport is the amount of overlap. The charge should be at least under two gates. To reach a sufficient overlap, a duty cycle of 5:8 is used. To achieve the typical well capacity Q_{max}, it is necessary to transport the charge no faster than the typical transport speed as specified in the data sheet. Exceeding the maximum frame transport frequency decreases Q_{max} considerably.

Figure 8: Waveforms of A and C clocks during image-to-serial transport

Figure 8 shows the waveform of the A and C clocks during the image-to-serial transport of the last image line. As can be seen, at this time C3 is 'low', separating charge from neighbouring columns; while C1 and C2 are 'high' to accept the charge packet.

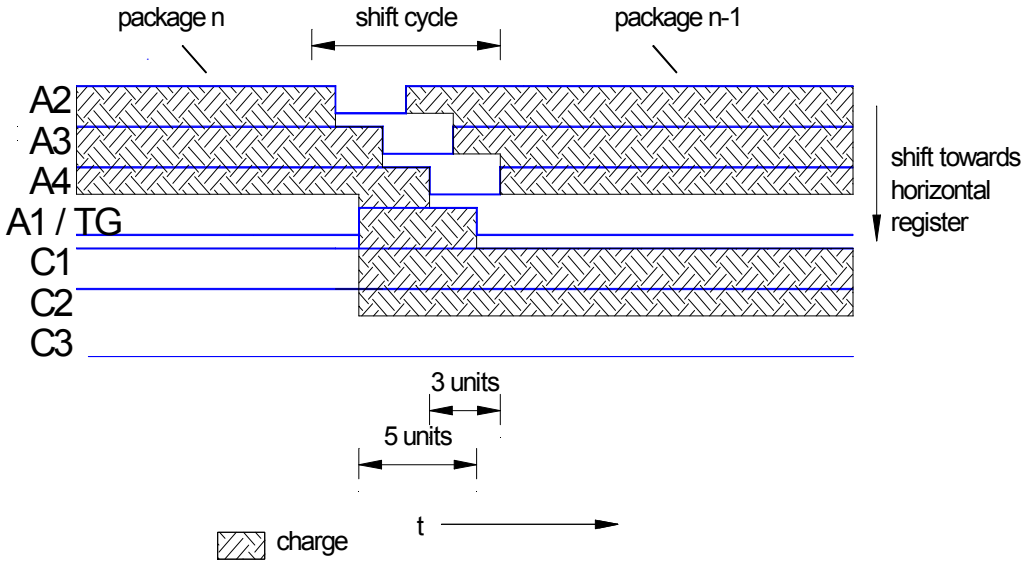


Figure 8: Waveforms of A and C clocks during image-to-serial transport

Figure 9 shows the waveform of the C clocks at the end of the image-to-serial transport of one line, and the start of the horizontal transport at 25MHz.

During readout the duty cycle used for the horizontal transport is 50%. This means that for 3 units the pulse is high; for the other 3 units it is low The essence here is that the time that the charge packets are under two adjacent gates should not be too short (overlap).

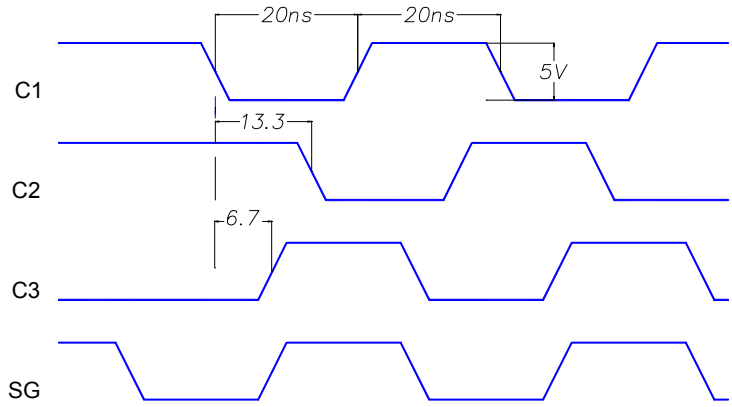


Figure 9: Waveform of C clocks at the start of the horizontal transport at 25MHz

Figure 10 shows SG clock together with the RG pulse. Notice that the rising edges of both signals start at the same time. The driver of RG is described in chapter 4.3

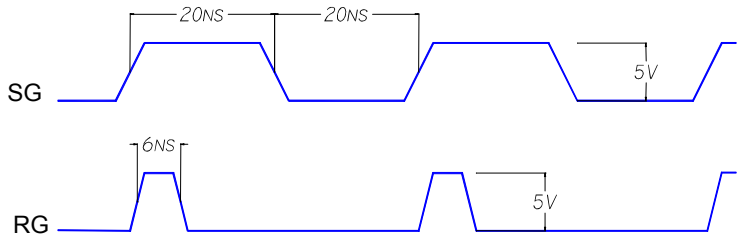


Figure 10: SG and RG waveforms

Figure 11 shows the output waveform of the CCD at the end of the active pixels of one line. The reset gate pulse causes cross-talk on the output signal of the CCD.

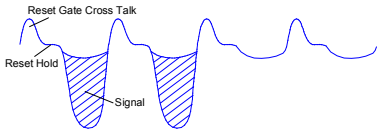


Figure 11: Output waveform of CCD

3.4. Readout mode

Only single output readout mode of the CCD's is explained in this application note.

3.4.1. Shot mode

In full resolution shot mode, a mechanical shutter is required to obtain a 100% smear-free image. After integration, the shutter closes. Then the line-per-line readout starts.

4. Application Circuit

Figure 12, Figure 13, Figure 14 and Figure 15 show the recommended way to drive the different sensors. Three types of input signals can be identified:

- DC Bias Supply (From V-Driver, TDA9991)
- Vertical Inputs (From V-Driver, TDA9991)
- Horizontal Inputs (From PPG, SAA8103)

4.1. DC Bias Supply

Most of the DC Bias voltages are derived from SFD. Therefore only two DC Bias supplies are needed. One supply for VNS, the other for SFD and others (VPS, RD, OG, RG SG and C gates). Not only is this the easiest solution, it's also the safest.

The Vertical Driver was designed in such a way that sufficient current can flow in normal operation. Excessive currents during power-off or power-on, or destructive latch-up, are not possible.

VNS and SFD are adjustable via software. VNS is set (between 20V and 28V) to have good anti-blooming behavior. SFD is normally set to 20V.

4.2. Vertical Inputs

The image gates (A1, A2, A3, A4 and TG) are driven from a low resistance source with a clock swing of 8V during integration and 11V during vertical transport. The dedicated V-Driver chip is the TDA9991 (See also 5). The vertical waveforms generated by the PPG are to be converted from logic levels to 'Image gate' levels.
The Electronic Shutter (ES) or Charge Reset (CR) signal resets the image. A voltage swing of 5V is sufficient (also supplied by the V-driver).

4.3. Horizontal Inputs

For the horizontal clocks a separate driver must be used. The best choice for this purpose is a 74ACT04, which accepts logic (TTL) levels.
Gates C1, C2, C3, RG and SG are direct outputs of the 74ACT04 driver and need to be clamped to a DC value derived from VSFD.

4.4. Emitter Follower

The CCD output buffer has an open source output and should be loaded with a resistor to GND. In order to prevent bandwidth limitation as a result of capacitive loading, an emitter follower with a high-frequency transistor should be used.
It is essential to mount the emitter follower (including by-pass capacitor) as close as possible to the output pin and keep the connection between emitter and the next stage as short as possible in order to minimize any stray capacitance to GND.

The CCD output buffer can easily be destroyed by ESD. By using this emitter follower, this danger is suppressed.

☞ Measuring directly on the output pin of the sensor with an oscilloscope probe can easily damage the output buffer. To avoid this, measure on the output of the emitter follower instead.

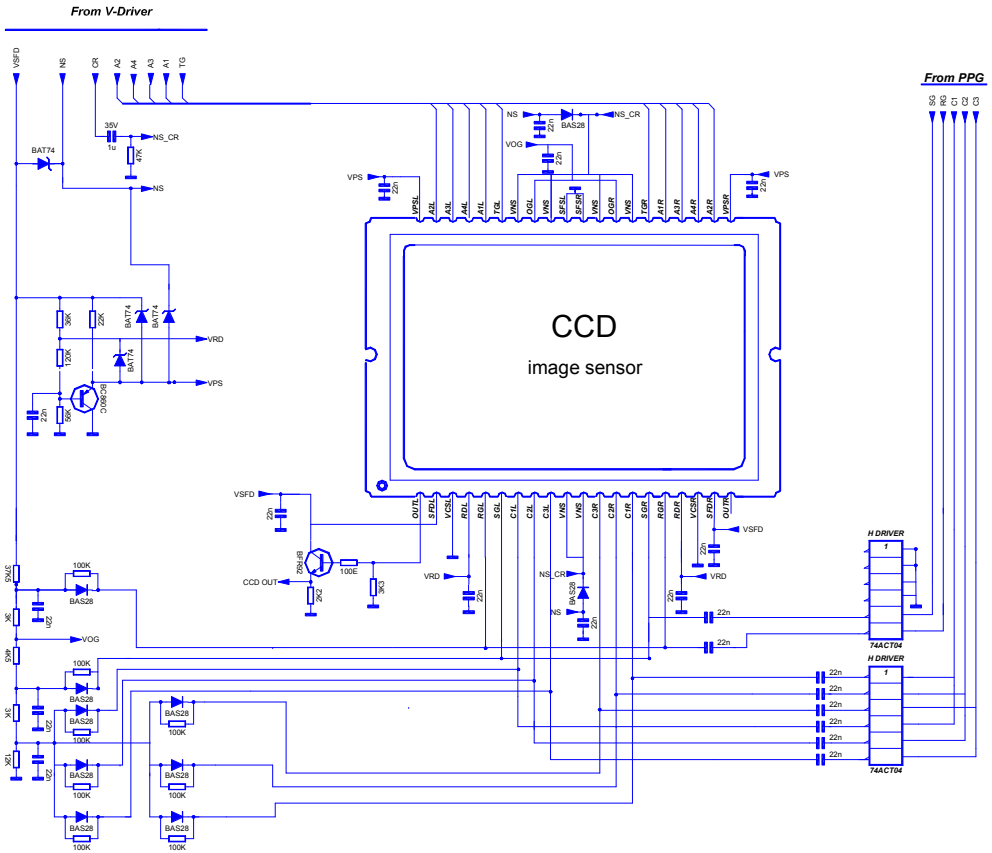


Figure 12: FTF2416 sensor application

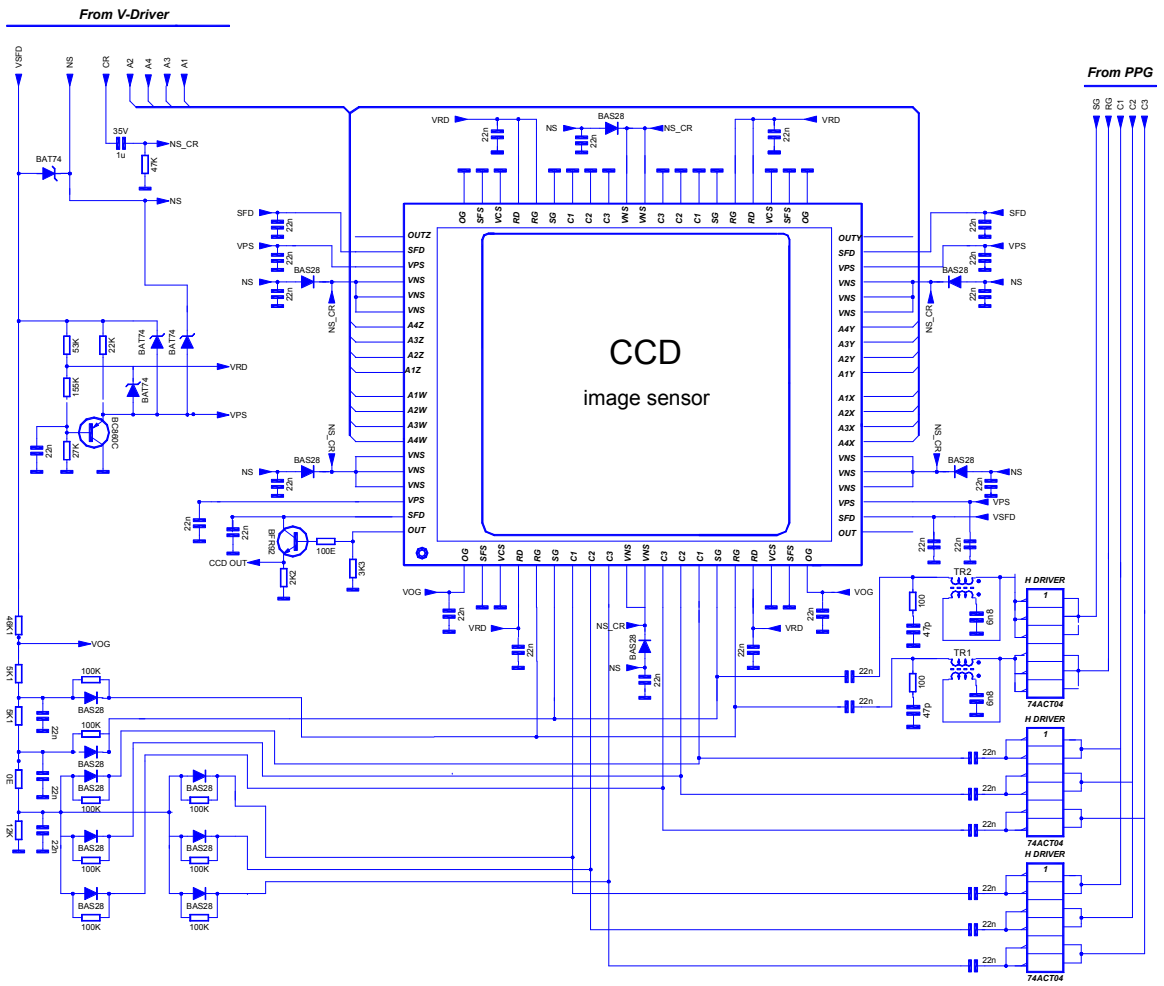


Figure 13: FTF2020 / FTF3020 / FTF7040 sensor application

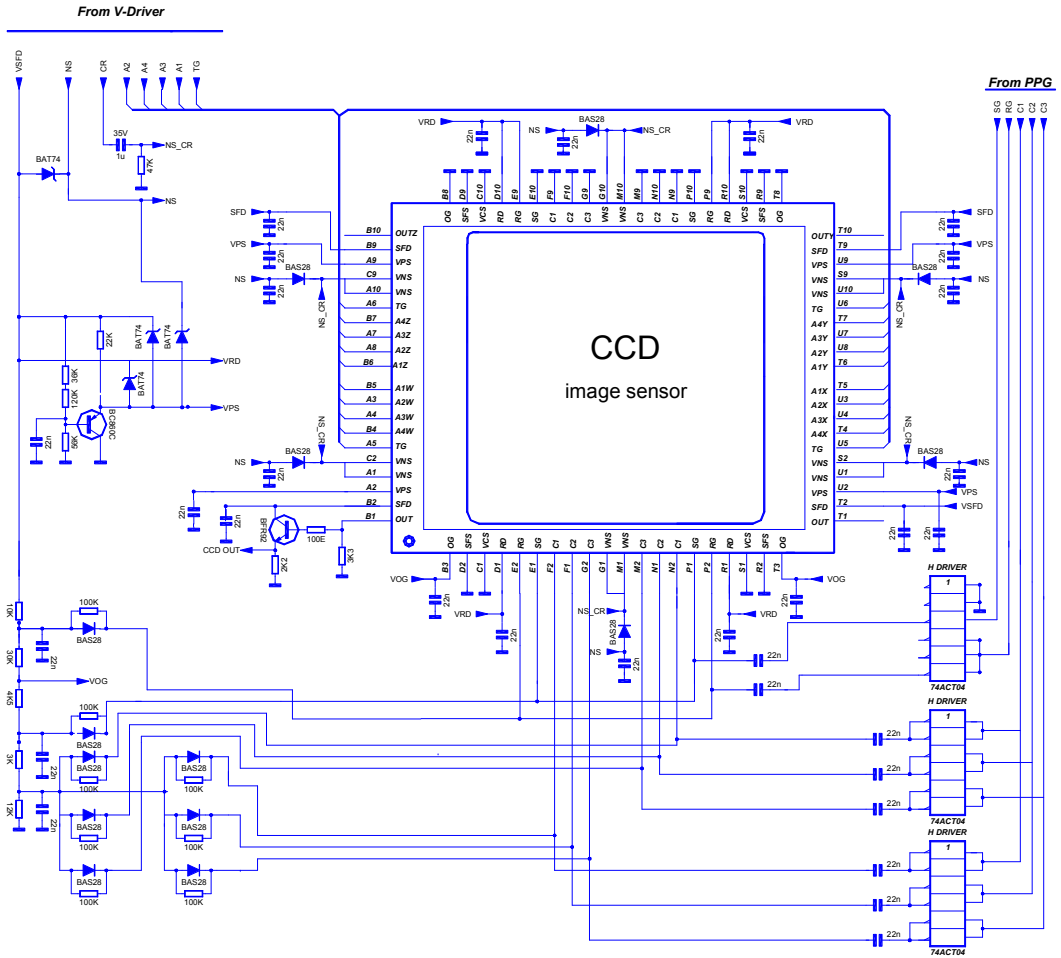


Figure 14: FTF4027 / FTF4052 / FTF5033 /FTF5066 sensor application

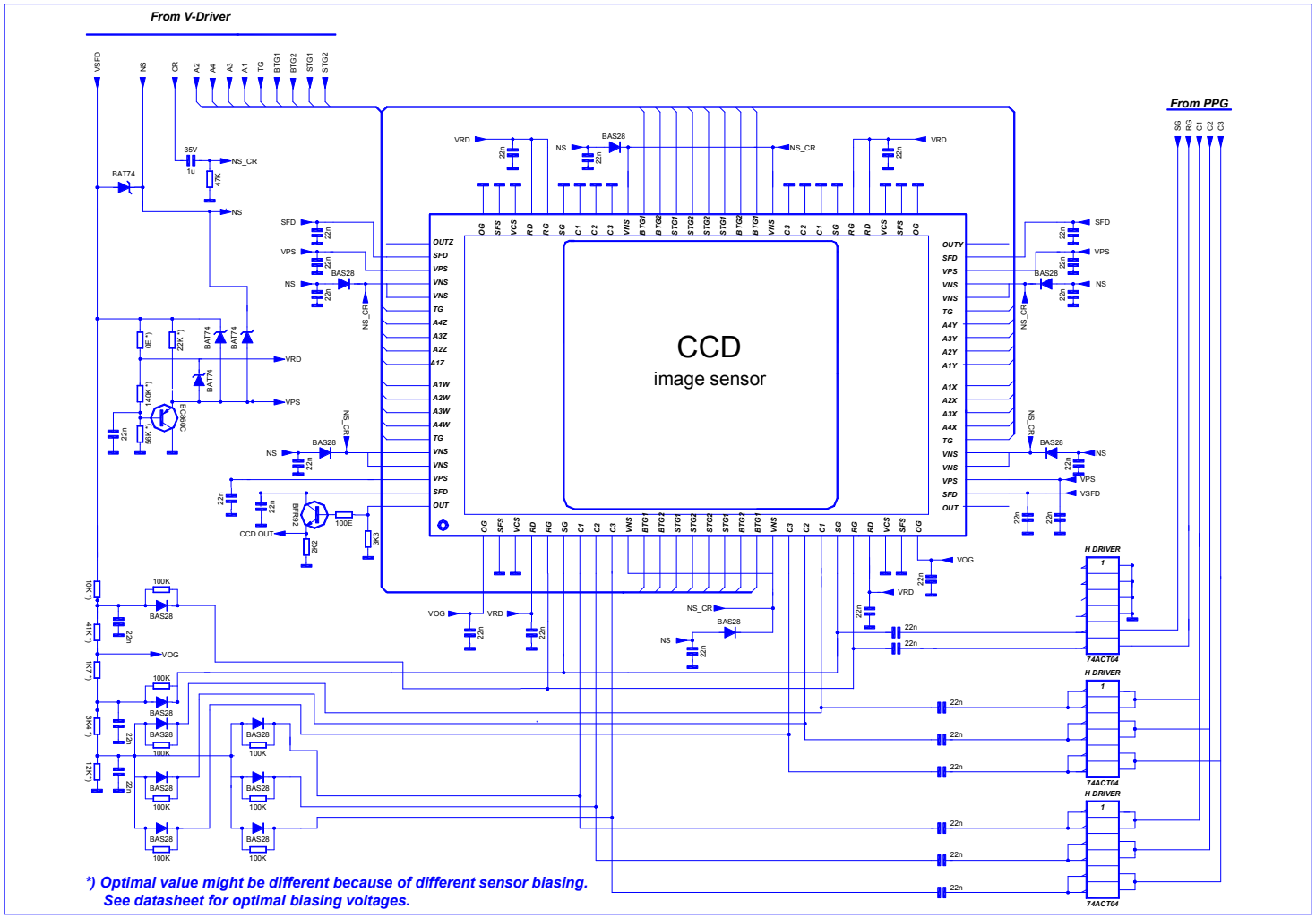


Figure 15: FTF6146 sensor application

5. Pulse Pattern Generator SAA8103

5.1. General

The SAA8103 is a PPGFT (Pulse Pattern Generator for True Frame CCD) for use in Digital Still Camera systems. This IC generates the driving pulses for the CCD. This IC generates the signals for driving the CCD, in combination with the V-driver IC (TDA9991) and also generates the pulses for the pre-processing part, CDS and ADC (for instance the AD9824). It also generates synchronisation signals HD and VD, reference signals HREF and VREF for the rest of the system.

The PPGFT can be locked with external synchronisation signals (HD and VD). Each drive signal that will be generated will be synchronised with the external HD and VD signals.

Two different read-out modes for the CCD can be programmed: Shot mode and Preview mode. Shot mode is used for taking a full frame shot. Preview mode is used for video-monitoring. Preview mode is not implemented for full frame CCD's

The PPGFT also supports the electronic shutter function. Exact setting of integration time can be programmed.

The PPGFT runs on an internal main oscillator from 6 - 28MHz by selecting a X-tal. For this application note the PPG runs at 25 MHz.

The vertical drive signals are connected to the TDA9991. Horizontal drive signals are connected to the CCD via 74ACT04 logic drivers. Sample-hold and clamp pulses are provided for the pre-processing part, CDS and ADC (for instance the AD9824), synchronisation signals (HD and VD) or reference signals (HREF and VREF) are provided for Camera system.

These pulses are controlled with a microcontroller via serial interface (I2C or SNERT). The PPGFT receives address and data of I2C or SNERT, and decodes these inputs for internal logic. It also decodes these inputs for the serial interface of AD9824 and TDA9991.

Setting-files needed to operate the PPG can be obtained on request from DALSA Professional Imaging

In this case the following information is needed:

1 CCD layout structure (pixel map).

2 Application (which read out modes are needed)

3 Peripheral IC's used (frontend type, u-controller, master-slave configuration)

For application diagram see Figure 16.

5.2. Control

The PPGFT receives its addresses and data by I2C or SNERT. This data is decoded for generating the defined pulses. Also the control data of TDA9991 and AD9824 is decoded and supplied by serial interface to these devices.

5.3. Pulse Pattern Generator (PPG)

Two different types of pulses are generated by the SAA8103.

5.3.1. Low frequent pulses

Low frequent pulses are defined and generated with a resolution of 1 pixel period.

VA1, VA2, VA3, VA4 and TG are the input signals for the V-driver to drive the image clocks.

VTLVL is the pulse that controls the level switching of the image clocks when 3-level image clocks are used.

CR is the Charge Reset pulse that is an input of the V-driver.

CLP1 and CLP2 are two clamp pulses for clamping the black lines and/or black pixels in the frontend (AD9824) to obtain the proper black level out of the camera.

VD and HD are synchronization signals. They can be used to synchronize the camera to external synchronization signals or they can be used as reference signals for the camera system.

TRG can be used to trigger the integration time to an external trigger signal.

5.3.2. High frequent pulses

High frequent pulses are defined and generated with a resolution of 1/24 pixel period.

5.4. Mode of operation

Two different integration modes can be implemented with the SAA8103.

1. Stand-alone mode: In this mode the start of integration and integration time is set by PPG.
2. Triggered slave mode: In this mode the start of integration and integration time is set by the trigger input signal.

For detailed information: see datasheet and application note of SAA8103 on DALSA website.

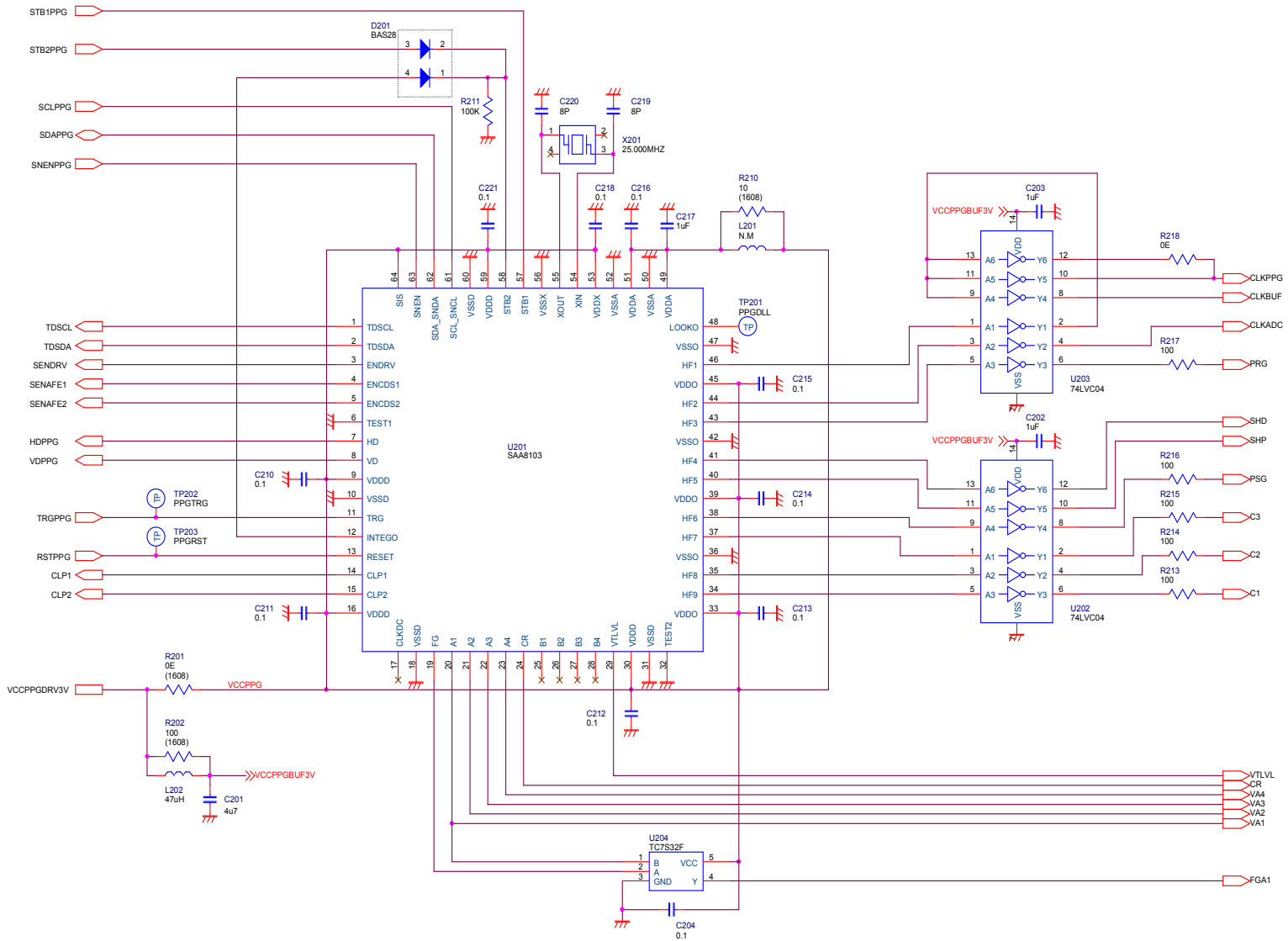


Figure 16: SAA8103 application

6. V-Driver TDA9991

6.1. General

The TDA9991HL forms the interface between the PPG and CCD image sensor in camera-systems and minimizes the component count by integration of various functions. The IC contains eight vertical line drivers, a shutter-driver for charge reset, a versatile programmable DC-DC converter, a non programmable DC-DC converter and voltage regulators which create all required low noise supply voltages for FT CCD sensors. A three wire serial bus is used for programming the device. The versatile programmable DC-DC converter generates two positive voltages (CAPNS, CAPH). Voltage regulators convert the DC-DC converter outputs CAPNS and CAPH into low noise output voltages (VNS, VSFD, VH, VSH). The required voltages for the image sensor and the drivers can be programmed via the serial bus with sufficient accuracy to optimise the performance of the sensors. An on board reference ensures stable output voltages over the entire temperature range. An internal DCOK signal enables the vertical line drivers when the DC-DC converter output voltages and the output voltages of the voltage regulators are at their required (programmable) level. When either VH, CAPNS or VNS drops below 80% of it's programmed level DCOK will become low. A START signal (inverse of DCOK) signalling that the device is starting up is externally available. The use of two external coils enables high efficiency of the DC-DC converters and fast start-up. The maximum current built-up in coil L2 (see figure 1 of datasheet) can be set with an external resistor (RLIM, resistor on pin-9) optimising efficiency of the DC-DC converter and making it independent of supply voltage (VDD) variations. The DC-DC converter can be operated with an on chip free running oscillator. The low impedance of the drivers enables fast transfer of the image of the sensor. The drivers can switch between zero and VH (8V to 15V). The 8 image gate drivers can be put into tri-state via the serial bus. Charge reset can be performed with a separate electronic shutter (ES) driver. In power down (can be set via serial bus) the current consumption (IDDQ) becomes virtually zero. The serial bus is still available.

For more detailed information see datasheet on DALSA website.

6.2. Level switch

To obtain a higher linear output signal (Qlin) out of the CCD's, 3-level image clocks are supplied. This means during integration the level of the image clocks A2, A3 and A4 is 8V (Level of blocking gate A1 is 0V) and during vertical transport the level is 11V. During charge reset all image clock levels are 0V. For implementation of a level switcher see Figure 17. The level during transport is set through the V-driver by software. The level during integration is set by resistor R433, R436 and R439. Switching is controlled by pulse VTLVL. The network with U438 and resistors, diodes and capacitors is to avoid cross conductance between Q430, Q431, Q432 and Q433.

6.3. SFD buffer

In Figure 17 for SFD an additional buffer is applied. This is only needed when the required current of SFD is > 20 mA. For a single output application the required current of SFD will be less then 20 mA. For these applications the additional buffer can be skipped and replaced by the filternetwork.

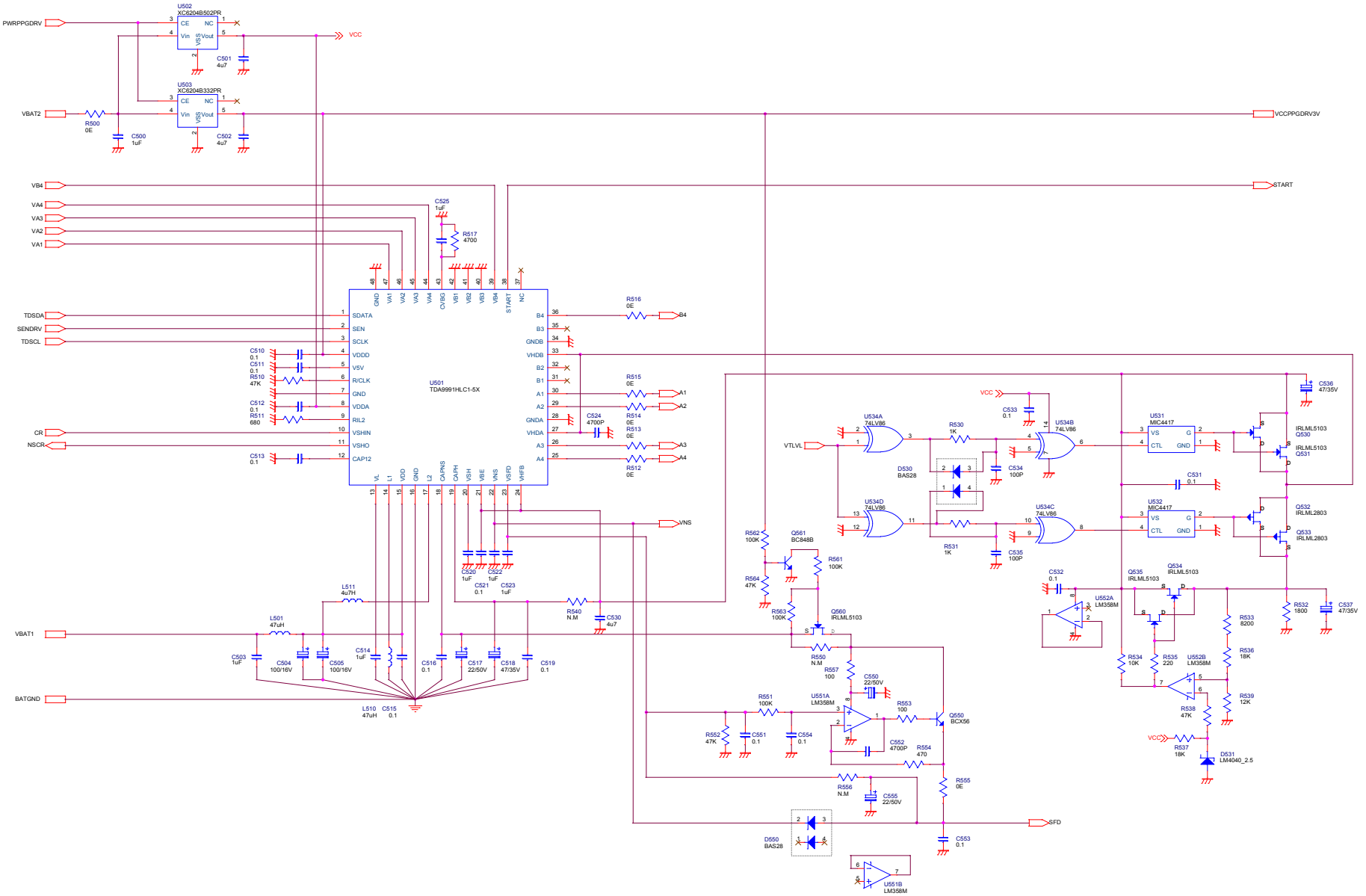


Figure 17: TDA9991 application

7. CCD signal processor AD9824

7.1. General

The AD9824 is a 14-bit analog-to-digital interface for CCD cameras. It converts the sensor output signal into a 14-bit digital signal. The device includes a Correlated Double Sampler (CDS) circuit, Pixel gain amplifier (PxGA), Variable Gain amplifier (VGA) and a low-power 14-bit Analog to Digital Converter (ADC) together with its reference voltage regulator. Low noise clamp circuits control the ADC input clamp level. The AD9824 also contains an analog preblanking function and an auxiliary input with VGA and input clamp. The device is controlled by 3-wire serial digital interface. The AD9824 can be ordered at the distributors of Analog Devices.

7.2. Input pulses

The CDS operation needs two input pulses (SHP and SHD). SHP is active during the reset hold level of the sensor output signal. SHD is active during the signal period of the sensor output signal (See timingdiagram in datasheet of AD9824 for more details: http://www.analog.com).
The timing of SHP, SHD and CLKADC are strongly related to SG- and RG pulse of CCD. To avoid different delays between these pulses over the whole temperature range it is recommended to have the same number and same types of logic devices between the generation of these pulses and CCD and AD9824.

Two lineclamp pulses are needed. CLPDM is used for clamping the CDS circuit within its input range. CLPOB is used for clamping the optical black pixels to the required digital value which is set by the serial interface. CLPOB and CLPDM are active during the first black pixels per line which are coming out of the CCD.
CLKADC is used for clocking the ADC. (See timingdiagram in datasheet of AD9824 for more details)
HDPPG and VDPPG are needed when the pixelgain (PxGA) function will be used.

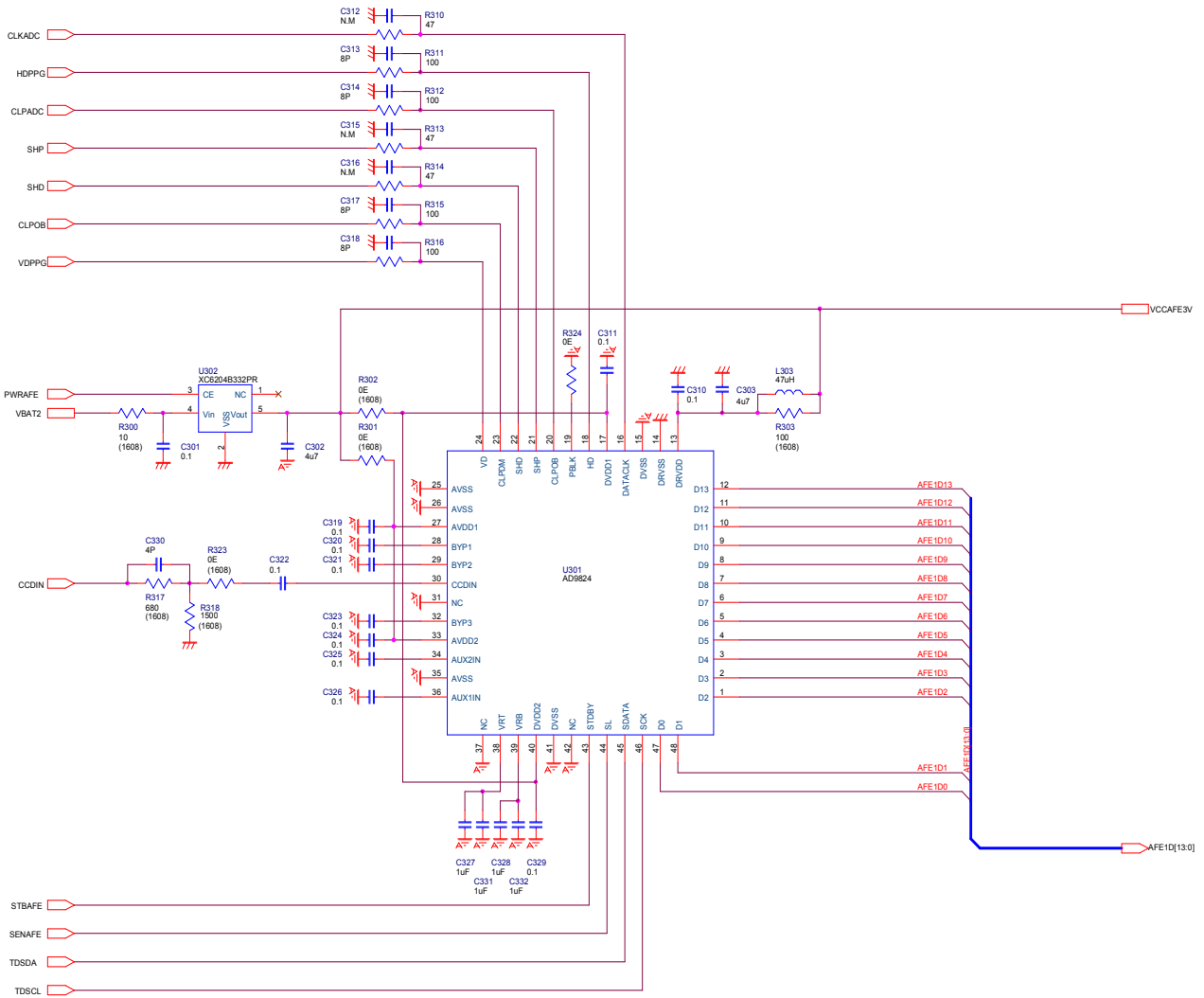


Figure 18: AD9824 application

8. Powermanagement

Power management is an important item in Digital Still Camera's. The DSC is battery operated so power-saving operation is necessary.

The used IC's do all have the possibility to operate in a standby mode where the dissipation is minimized.

To get the highest efficiency VBAT should be connected directly to the TDA9991. The power-off current is smaller then 4µA, so the battery-lifetime is not affected with this direct connection.

8.1. Power control options

8.1.1. Power control options of SAA8103 (PPG)

The PPG has two standby-pins. With these standby pins, the some circuitry including the HF outputs can be frozen. This makes the dynamic power load due to these outputs zero. The PPG core will still be running when the standby pins are activated. The load of the PPG is approximately 35mA, however if the outputs are connected to switched off circuitry, they may have a DC load (protection diodes at digital inputs) that can be multiples of this value. In standby settings can be loaded to the PPG and the 3W-interface to the CDS & V-driver can still be used.

There are two pins, which makes it possible to define which HF outputs are frozen. If the pin assignment is well done, it is possible to control the HF signals to the CCD and the CDS separately. See Figure 16 for the optimal pin assignment.

The read-out delay function (register 95 dec.) is used for power control. The microcontroller is used to keep the Front-End and horizontal buffers in standby during integration. The read-out delay is used to extend the integration time. This makes it possible to switch the CDS and buffers on *before* the CCD integration time is finished.

8.1.2. Power control options of TDA9991 (V-driver)

The V-driver has two power inputs, the DC/DC converter high power input VBAT (3.6…7V). This has almost no leakage current and can be connected directly to the battery. The other inputs have a low consumption and a higher standby current. For the V-diver 3 power states are defined:

- Off (<4uA): Only Vbat is applied, the other supplies are floating (or low)
- Standby (<400uA): All supplies are supplied, but the device is put into standby mode
- On (150..400 mA): the device is fully active

In Standby function, the settings can be loaded and are kept. The standby mode can be set via the serial interface that is also used to load the settings.

If more then 20mA is consumed from SFD, an external buffer is required.

Power control options of AD9824 (Front-End)
This frontend has a single standby pin that switches off almost the entire device. In standby mode, the settings can still be loaded.

For the Front End 3 power states are defined:
- Off: All supplies are floating (or low)
- Standby (4mA: All supplies are supplied, but the device is put into standby mode)
- On (ca 100 mA): the device is fully active

☞ For up-to-date information about powermanagement please contact DALSA Professional Imaging Application Support.

9. Critical design issues

The components of this design must be carefully placed on the pcb. Some components have critical signal paths which should be carefully designed.

☞ DALSA can give full support with reviewing schematics and pcb-layout.

The analog paths from CCD-out to the input of the AD9824 have to be as short as possible. Keep analog and digital grounds separated.

The TDA9991 layout can be critical. The DC-DC converter parts have to be compactly placed and have to be connected as direct as possible to the battery terminals. The inputs of the DC-DC terminals are designed to handle four pen-lite batteries (voltage range is from 3.6V up to 7V).

For more up-to-date description on board layout of TDA9991: Please contact DPI Application Support

9.1. Power and grounding recommendations

When designing a printed-circuit board for an application such as digital still cameras, care should be taken to minimize the noise. For the front-end integrated circuit, the basic rules of printed-circuit board design and implementation of analog components (such as classical operational amplifiers) must be respected, particularly with respect to power and ground connections. The following additional recommendation is given for the CDS input pin(s) which is/are internally connected to the programmable gain amplifier.

The connections between the CCD interface and CDS input should be as short as possible and a ground ring protection around these connections can be beneficial.
Separate analog and digital supplies provide the best solution. If it is not possible to do this on the board then the analog supply pins must be decoupled effectively from the digital supply pins. If the same power supply and ground are used for all the pins then the decoupling capacitors must be placed as close as possible to the IC package.
In a two-ground system, in order to minimize the noise through package and die parasitics, the following recommendation must be implemented. All the analog and digital supply pins must be decoupled to the analog ground plane. Only the ground pin associated with the digital outputs must be connected to the digital ground plane. All the other ground pins should be connected to the analog ground plane. The analog and digital ground planes must be connected together at one point as close as possible to the ground pin associated with the digital outputs. The digital output pins and their associated lines should be shielded by the digital ground plane which can then be used as return path for digital signals.

10. Golden Rules

For a successful design be aware of the following rules.

- Make sure you fully understand the operation of the CCD including the function of each pin.
- Consider all of the horizontal clocks as analog circuits since any noise on these signals will be visible in the output signal. This means that phase noise caused by cross-talk of any other signal (especially with a lower frequency) should be avoided. For this reason it is recommended that the horizontal clock circuitry is isolated from the rest of the electronics.
- Make sure the rise and fall times of all transport clocks (both horizontal and vertical) are fast enough. Too slow clock drivers result in a too short overlap time. This leads to a deterioration of the charge transport efficiency, yielding a lower Qmax. Typical effects of slow horizontal clock drivers are bad pixel separation or vertical stripes.
- Don't re-invent the wheel. Many engineers have spent years on developing high performance cameras. This has resulted in a camera set-up as presented in this note. Of course, one is free to use other circuits or components, as long as it basically has the same functionality.
- Protecting the camera from unwanted differential voltages is an essential part of a camera design. Be aware of the safe startup sequence of all CCD signals. Here's the sequence:
  1. SFS (if not connected to GND)
  2. VNS
  3. SFD
  4. VRD
  5. VPS
  6. the rest

  The voltage difference between VSFD and VRD must not exceed the 5V during switching on and off of the camera.

  This does not mean that VNS should be stable before VSFD can be switched on. As long as the VNS voltage is a minimum of 1V higher than VSFD. Deriving all sensor bias DCs has the advantage that this law isn't violated. When switching off the camera, remove the signals in reverse order.

  Do not exceed the maximum voltage difference between the biasing voltages that are mentioned in the datasheet of the CCD's.
- Be sure you read the section on layout design. No matter how good your schematics are, a poor layout design will definitely lead to a disappointing performance.
- The performance figures are valid for the typical values mentioned in the data sheet. To obtain maximum performance use the specified bias voltages and waveforms.

- In many cases only one output register and one output buffer are used. For safe operation, connect the **unused output buffers and output register** pins as follows:

Pin	Connected To
RG	Reset Drain voltage
SG	GND
C1..3	GND
VCS	GND
RD	Reset Drain voltage
SFD	VSFD
SFS	GND
OG	VOG
Output	Not Connected

11. DALSA Professional Imaging Application Support

DPI application support can be obtained at the following facilities. In Japan, please contact our Tokyo office. For other areas please contact our Netherlands office.

Global

High Tech Campus 27
M/S 01
5656 AE Eindhoven
The Netherlands
Phone: +31-40-259-9067
Fax: +31-40-259-9005

Japan

Suite 1301
3-4-3 Higashi-Ikebukuro,
Toshima-Ku Tokyo
Phone: +81-3-5960-6353
Fax: +81-3-5960-6354