CMOS vs. CCD:

Maturing Technologies,Maturing Markets

The factors determining which type of imager delivers better cost performance are becoming more refined.

by Dave Litwiller, Dalsa

CCD and CMOS image sensor technologies were invented in the late 1960s and early 1970s. At the time, CMOS performance was limited by available lithography technology, allowing CCDs to dominate for the next 25 years.

The original argument a decade ago for the renewal of CMOS image sensors as a competitor to CCD technology was generally based on several ideas:

1. Lithography and process control in CMOS fabrication had reached levels that soon would allow CMOS sensor image quality to rival that of CCDs.
2. Integration of companion functions on the same die as the image sensor, creating camera-on-a-chip or system-on-a-chip capabilities.
3. Lowered power consumption.
4. Reduced imaging system size, as a result of integration and reduced

CCD and CMOS imagers will see continued growth in markets such as cell phones, automotive safety, authentication and security systems (see figure above).

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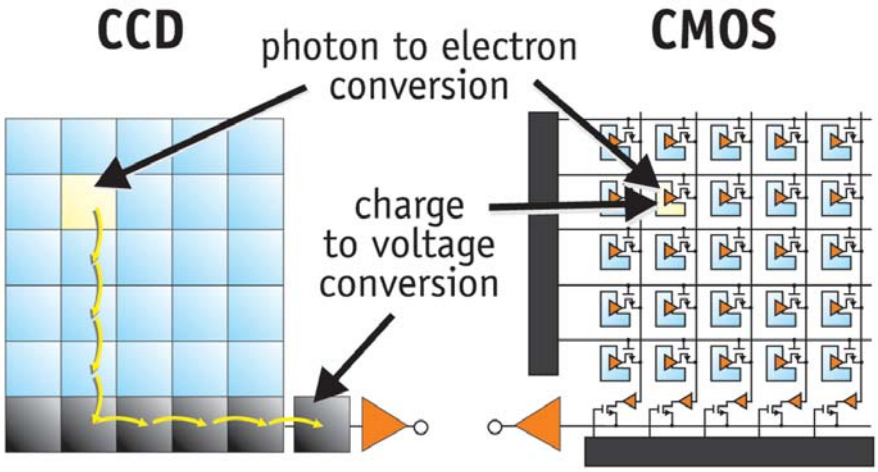
power consumption.

5. The ability to use the same CMOS production lines as mainstream logic and memory device fabrication, delivering economies of scale for CMOS imager manufacturing.

Other conventional arguments favoring CMOS included operation with a single power supply, and the ability to do region-of-interest, or windowing-read-outs, with the imagers.

A great deal has changed with CMOS and CCD technology. Some projections turned out to be true. Others have changed with an evolving technology landscape. Today there is a vibrant industry for both types of image sensors. Structural changes in the technology and business environment mean that a new framework now exists for considering the relative strengths and opportunities of CMOS and CCD image sensor technology.



CCDs move photogenerated charge from pixel to pixel and convert it to voltage at an output node. CMOS imagers convert charge to voltage inside each pixel.

Straight path for CCDs

CCD technology has undergone incremental advances in device design, materials and fabrication technology. CCD image sensors have steadily increased in quantum efficiency, decreased in dark current and in pixel size, reduced operating voltages (power dissipation) and improved signal handling. And their companion circuits have become more integrated, making CCDs easier to use and allowing faster time to market. CCDs now yield better performance with less power and reduce the size of camera systems.

Today, CCDs have a prominent role in high-volume uses, such as cellular phones, camcorders and consumer digital cameras, as well as high-performance applications such as professional photography and industrial, scientific, medical and military/aerospace deployment.

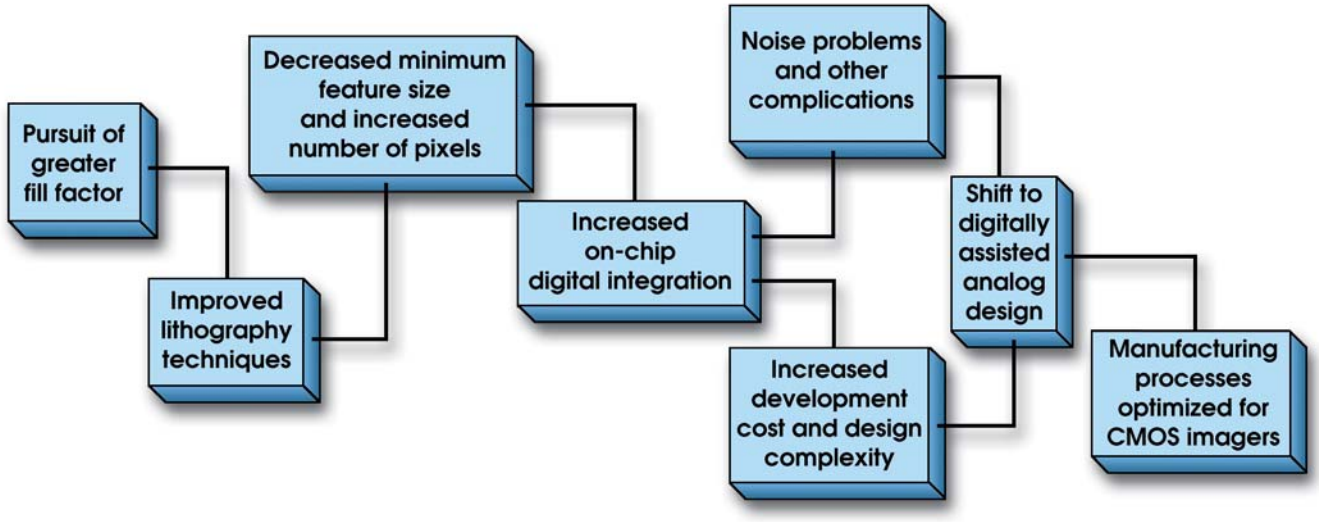
Winding road for CMOS

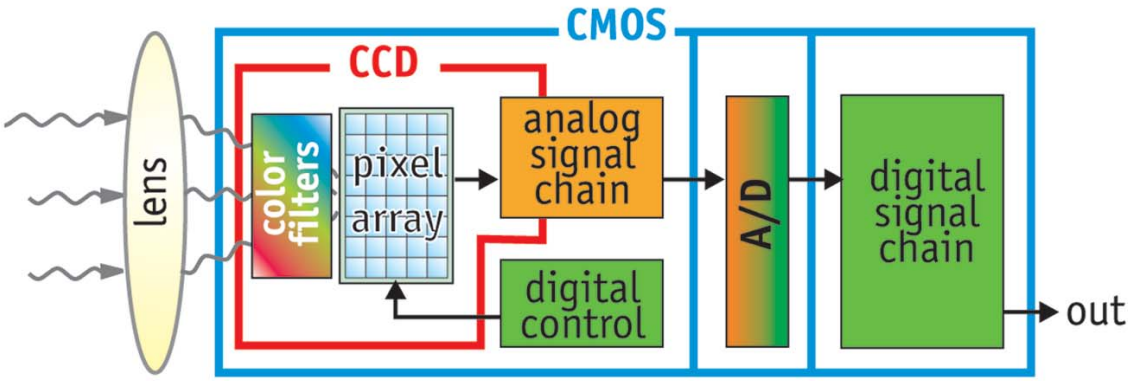
Compared with CCDs, the recent progress of CMOS imager technology has been more rapid, yet more turbulent. Arguably, the journey toward better performance in CMOS image sensors began with improving fill factor.

The desire for performance and flexibility in pixel architecture in imagers competes with the amount of space in each light-sensing pixel because CMOS imagers generally require a number of optically insensitive transistors in each pixel.

The pursuit of greater fill factor and the related ability to produce smaller pixels has improved the min-

The Road to Today's CMOS Imagers





CMOS imagers can be fabricated with more "camera" functionality on the chip. This offers advantages in size and convenience.

imum feature size of 0.5 µm and larger of a decade ago. CMOS imagers have gone from fabrication process technology of 0.35 and 0.25 µm to 0.18 µm in the most advanced devices and, in a growing number of cases, even smaller. Advancing lithography technology to improve fill factor and optical sensitivity increased the opportunity for digital integration on the chip because smaller transistors decrease both power dissipation and the die size that are needed for integrated circuit functions.

However, CMOS technology's dependence on advancing lithography came at a price. Progressively denser lithography increased development costs — in large part, because of rising reticle costs at each fabrication technology node. And, although smaller transistor sizes facilitate digital integration, integration often increases design complexity faster than design productivity.

Design complexity outpacing design productivity for leading-edge integration on a very large scale placed a rising cost burden on progressively deeper submicron CMOS image sensor designs, especially those with increasing digital on-chip integration.

Substantial on-chip digital integration can also bring with it noise coupling issues, with switching transients introducing noise into analog signal pathways and even into some digital ones. Noise coupling of digital integration can conflict with the pursuit of image quality. Design complexity, design cycle duration and noise have often meant that digital integration generally has not been able to take full advantage of the lithographic trajectory of CMOS image sensors.

A more significant and unavoidable challenge of deep submicron image sensor design in CMOS sensors is the analog portion of the integrated circuit. As microelectronics fabrication technology becomes

Initial Prediction for CMOS	Twist	Outcome CMOS vs. CCD
Equivalence to CCD in imaging performance	Required much greater process adaptation and deeper submicron lithography than initially thought	High performance available in both technologies today, but with higher development cost in most CMOS than CCD technologies
On-chip circuit integration	Longer development cycles, increased cost, trade-offs with noise, flexibility during operation	Greater integration in CMOS than CCD, but companion ICs still often required with both
Reduced power consumption	Steady progress for CCDs diminished the margin of improvement for CMOS	CMOS ahead of CCDs
Reduced imaging subsystem size	Optics, companion chips and packaging are often the dominant factors in imaging subsystem size	Comparable
Economies of scale from using mainstream logic and memory foundries	Extensive process development and optimization required	Legacy logic and memory production lines are commonly used for CMOS imager production today, but with highly adapted processes akin to CCD fabrication

denser, analog circuit performance typically suffers. For 0.25-µm technology and smaller, supply voltages drop from 5-V levels, introducing constraints on dynamic range at the signal levels relevant to most image sensors. Below 0.35 µm, linearity of transistor performance also tends to diminish.

Declining linearity and dynamic range combine to erode the accuracy of analog circuitry. Other analog performance complications, such as leakage current and complementary circuit matching issues, can arise with increasingly dense fabrication technologies.

Fighting the decline of analog performance in deep sub-micron CMOS required a significant shift in sensor and circuit design. The technology shifted to digitally assisted analog design, which repartitions analog and mixed signal circuit functions so that accuracy and some speed demands of traditional analog circuit elements are off-loaded to digital circuit blocks.

A common example is to divert speed-intensive operations to the digital domain, allowing related analog functions to operate at lower bandwidth and noise levels. Shifting accuracy and certain speed requirements to digital circuit elements can maintain or enhance significant aspects of overall CMOS image sensor performance.

However, because there were few relevant precedents for such high-performance digitally assisted circuit design from other applications, it has taken a number of years to develop digitally-assisted analog architectures that fully embrace all of the competing forces among design, electro-optical performance and fabrication of CMOS image sensors.

The fabrication process is a defining aspect of CMOS sensor performance and has evolved considerably. From an initial notion of reusing or lightly adapting standard logic or memory processes, there has been an iterative journey to optimized CMOS image sensor processes. These process technologies have often become complex in terms of the number of mask layers and process steps to meet all competing requirements.

The movement of CMOS image sensors away from standard memory or logic fabrication processes started with changes to silicides and dielectrics to improve optical compatibility. Further changes have been made to:

- Reduce the optical stack height and improve its structure, thus enhancing quantum efficiency, off-axis image quality and color fidelity.
- Introduce pixel implants and deep depletion regions to control photodiode and Si-SiO_2 interface performance, influencing leakage (dark) current and image lag.
- Simultaneously manage analog and digital transistor properties as well as interconnects.

Concurrently optimizing electro-optical, analog and digital performance to the levels required for high-volume image sensor usage has been an expensive proposition. The lithography progression to smaller feature sizes has complicated matters further because some aspects of scaling for electro-optical and analog performance do not lend themselves well to parametric modeling or simulation. Process optimization at each lithography node typically requires experimentation and tweaking with real reticles and silicon, not just within a simulation environment.

The appreciable cost of process optimization in CMOS image sensor fabrication has shifted the advantage to manufacturers with captive foundries. Some "fab-less" players have been successful, but far more success stories have been fab-based. It has been easier for companies with fabs to customize the fabrication process because they have been able to maintain the attention of foundry process engineers.

There will continue to be viable roles for both fab-based and fab-less business models in CMOS image sensor development and production. However, the original notion of easy migration of production from one CMOS fab to another has given way to a far more cohesive and adapted relationship with a particular foundry, similar to that seen in the CCD industry.

CCD and CMOS technology

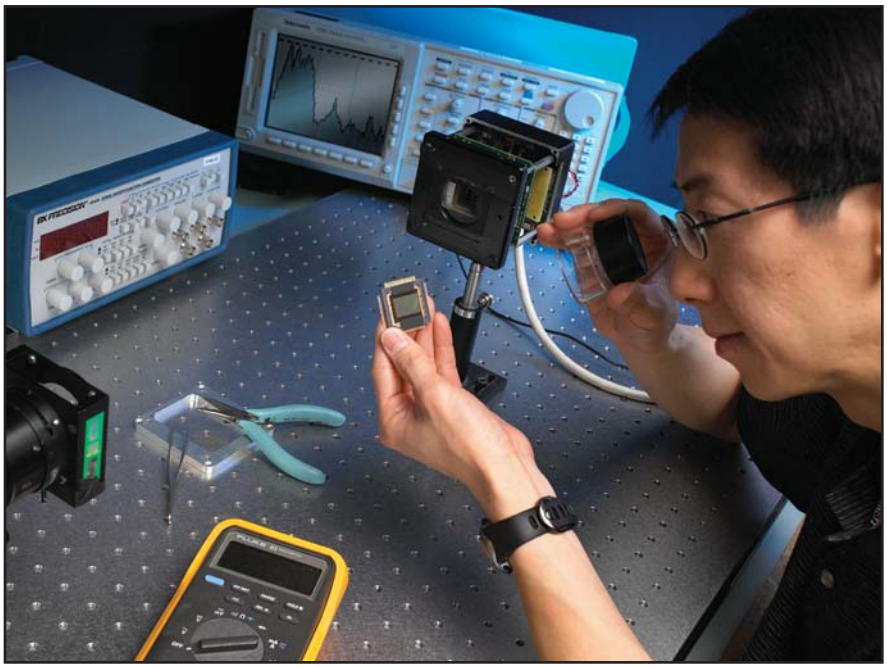
To reach the levels of performance needed for a variety of high-volume applications, CMOS image sensor pixel design and fabrication technology now more closely resembles that of CCDs than many people had predicted. Integration and power dissipation are decisive advantages of CMOS technology, whereas CCDs retain a greater ability for cost-effective adaptation and performance.

Contrary to the initial outlook, processed wafer costs have turned out to be less of an automatic advantage for CMOS. Wafer size, economies of scale and foundry-specific cost models, however, can be bigger factors favoring one technology over the other. Regardless of wafer size, the necessity of moving to deeper submicron technology for CMOS, for fill factor and other reasons, has delivered process control and cleanliness during fabrication (compared with less advanced fabrication processes) that can improve yield, particularly for large-die-area sensors.

CCD technology is not as lithography-dependent for its performance as CMOS technology. This statement is more strongly the case for line-scan, time-delay-and-integration and full-frame imagers, though still applicable for many electronic shuttering image sensor architectures. In general, achieving application-specific performance differentiation costs less with CCD technology than CMOS, both in sensor design and the fabrication process.

CMOS has made good on its promise of integration, low power dissipation and single-voltage-supply capabilities, and intensive iterative process engineering and device design have led to high image quality. CMOS technology, in part because of the migration to digitally assisted repartitioning of traditional analog circuit functions, has strength in high-speed imaging because of the relative ease of parallel readout structures in sensor implementations. Also, the flexibility in the technology for implementing electronic shuttering has leveled the playing field with interline-transfer CCDs.

The production cost per unit of processed silicon does not strongly favor one technology over the other (as originally thought). The extensive process engineering and number of fabrication steps to bring CMOS



Manufacturing and design of CCD and CMOS image sensors have changed significantly since they were invented.

image quality to levels comparable with CCDs required much more expensive wafer processing than was originally projected. Cost is often more strongly influenced by the business economics and competitive motivations of a particular foundry, rather than by the choice of technology itself.

There tend to be sharp differences in the wafer sizes used to manufacture CMOS and CCD image sensors, and the size depends on whether a manufacturer is fab-based or fabless and whether it is adapting a depreciated logic or memory production facility. There are more often third-party foundries available for 200-mm wafer production of CMOS image sensors, whereas CCD foundry production is frequently on 150-mm wafer lines. Captive production of CMOS and CCD imagers are done on 150-, 200- and 300-mm lines.

A larger wafer size reduces the labor cost per unit area of silicon processed. Thus, the availability of larger wafer sizes for CCD or CMOS can be a strong factor in the overall economics of production. The cost of manufacturing one or the other also depends on the type of wafer processing available and whether downstream sensor production volumes will carry the up-front development costs.

The road ahead

Over the past few years, the development of CMOS and CCD imager technology was driven in large part by the prospect of hundreds of millions of units in cell phones as well as the rise of consumer digital cameras. With both CMOS and CCD imagers designed into a large proportion of cell phones, and the digital photography marketplace coming to maturity, the question becomes: What will the next big markets be, and how will they shape imager technology?

It is unclear whether there will be another application comparable to cell phones for unit volume, but growth and advancement for image sensor technology will continue. Some of the largest forming waves include automotive and security. Automotive in-vehicle uses for imagers are rising, especially for safety systems. Sensors with onboard intelligence also are garnering increasing interest for security, surveillance, authentication and access control. These markets will likely stimulate further advances in sensor integration and ruggedness, with a major role for enhancements in packaging technologies as well.

There has been a significant shakeout in the image sensor marketplace over the past 10 years — more so for CMOS than CCD technology. Today, a more stable environment exists, which is of benefit to customers, employees and investors. Foment has given way to greater stability. Furthermore, at the levels of performance of both CMOS and CCD technology today — and the related skills in sensor test, assembly and packaging — the new markets for both image sensor technologies are likely to draw heavily on the capabilities of the incumbent producers, rather than more disruptive technology or application transitions that create periods of turbulence and new players. □

Meet the author

Dave Litwiller is vice president of Dalsa in Waterloo, Ontario, Canada.

Acknowledgment

The diagrams are courtesy of Albert Theuwissen and are from the white paper “Image Sensor Architectures for Digital Cinematography.”